SiT95901

Ultra Low-Power Dual I2C Real Time Clock (RTC)

Description

The SiT95901 is an Ultra-low power Real-Time Clock (RTC) and calendar device with Dual I²C bus supported.

SiT95901 support programmable time-of-day alarm and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The device registers provide seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The SiT95901 has a built-in a voltage-level detection circuit that detects power status and voltage level, when necessary, the device will automatically switch to the backup battery power supply (V_{BAT}).

Within battery (V_{BAT}) power supply standby mode, the device maintains time, date, and alarm operation with very low current consumption.

Dual I²C bus allow two master devices access to the device. the second I²C bus also can read/write most SiT95901 registers with the control bits set by primary I²C controller, The maximum data rate is 400 kbit/s.

Applications

- Server and computer precision timekeeping
- I/O controller Hub
- Products for unattended operation time
- Consumer products
- Industrial control

Features

- Real-Time Clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz MEMS oscillator or quartz crystal
- Support 24-hour and 12-hour Mode
- Support Daylight Saving Mode
- One time-of-day alarm
- Interrupt Flag Support
- RTC_CLR Flag
- Alarm Flag
- RTC Fail Flag
- Oscillator Fail Flag
- Battery-backed 128 byte SRAM
- Fast mode 400 kHz dual I²C-bus interface
- Device addresses
  - RTC: 1101 111
  - SRAM: 1010 111
- RTC_CLR# to clear Battery backed RAM
- Support Battery voltage level measurement
- Automatic power-level detect and switch circuitry.
- Oscillator's fail detection function
- Low current: typical 1 uA
- Programmable clock output for test and MFG (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)
- ESD protection
- 2 kV Human-Body Model (A114-A)
- 500 V Charged-Device Model (C101)
- Clock operating voltage: 1.55 V to 3.6 V
- Industrial temperature range (-40 to 85°C)
- Package offered: DFN12, 3 mm x 3 mm

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Block Diagram

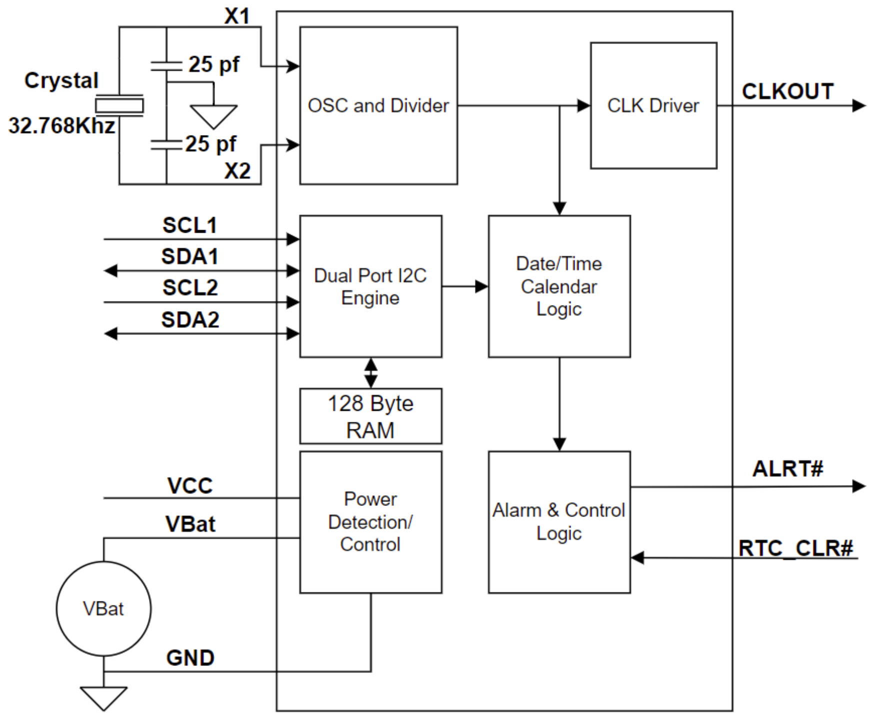


Figure 1. SiT95901 Block Diagram

3 x 3 mm Package Pinout

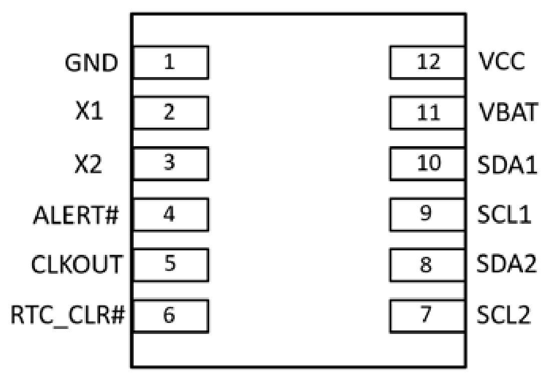


Figure 2. Pin Assignments (Top view)
(Refer to Table 1 for Pin Descriptions)

Ordering Information

SiT95901 A I - P

Part Family
"SiT95901"

Revision Letter
"A" is the revision of Silicon

Temperature Range
"I": Industrial, -40°C to 85°C

Packaging
"P": 4 ku Tape & Reel

Table of Contents

Device Configuration and Pin-out

Pin-out Top View

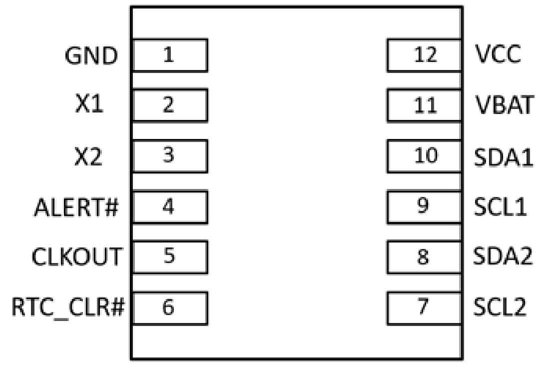


Figure 3. SiT95901 Pin Diagram

Table 1. Pin Description

Pin	Symbol	I/O	Function
1	GND	Ground	Ground pin
2	X1	I	Crystal input
3	X2	O	Crystal output
4	ALRT#	O	Low active Alert output (Open-drain output)
5	CLKOUT	O	Clock output
6	RTC_CLR#	I	Active low input to clear the internal memory, external pull up required
7	SCL2	I	Secondary I^2C bus Clock
8	SDA2	I/O	Secondary I^2C bus Data
9	SCL1	I	Primary I^2C bus Clock
10	SDA1	I/O	Primary I^2C bus Data
11	VBAT	Power	Backup battery power supply
12	VCC	Power	Main power supply Vcc for I^2C, Logical and Memory
	EPAD	Ground	Thermal pad should be connected to GND

Functional Descriptions

The SiT95901 is a dual I^{2}C interface low-current, Real-Time clock (RTC) timekeeping device, the device allows two external I^{2}C master devices (for example CPU and BMC) to individually access the calendar/data/time information.

The RTC chip contains 18 8-bit registers (00h~11h) and some reserved registers for testing purpose, an on-chip 32.768 kHz oscillator integrated, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calendar, and a dual port I^{2}C-bus interface with a maximum data rate of 400 kbit/s.

The built-in I^{2}C address engine will increment the register address automatically after each read or write of a data byte up to the register 11h, byte 12h~FFh is factory reserved registers for testing purpose. After register FFh, the auto-incrementing will wrap around to address 00h.

All registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The control registers (address 0Ah and 0Bh) are used as control and Dual I2C Port access right or sequency, status register.

Primary I^{2}C and Secondary I^{2}C

The primary I^{2}C interface operates or behaves like normal I^{2}C interface, the secondary I^{2}C interface write is controlled by TWO (Time-Register Write Ownership) bit which can be programmed by primary I^{2}C interface.

The primary I^{2}C can access RTC and SRAM including read/write on most of registers and control secondary I^{2}C on access rights.

The secondary I^{2}C could write to SRAM register (controlled by MWO bit) and CLK control register.

Both primary and secondary I^{2}C will be disabled during VBAT operation mode.

Normally, primary I^{2}C will be connected to CPU and secondary I^{2}C interface will be connected to EC or BMC device.

Device address of RTC and SRAM

The SiT95901 includes user RAM which can be accessed from primary I^{2}C and secondary I^{2}C controlled by SRAM Write Ownership (MWO) bit from primary I^{2}C permission. The I^{2}C addresses of RTC and internal SRAM are listed in Table 2.

Table 2. Device Address for RTC and SRAM

Device	I2C address in 7-bit
RTC	1101111
SRAM	1010111

Clock and Calendar

The time and date information are obtained by reading the appropriate register bytes. The time and calendar are set or initialized by writing the appropriate register bytes. Please refer to Table 2 register map of the RTC register details.

When the "ST" bit is set to 1, the oscillator divider is disabled. When set to 0, the oscillator divider is enabled. The clock can be halted whenever the timekeeping functions are not required, which decreases V_{BAT} current.

The day-of-week register increments at midnight.

Time and Date Operation

The SiT95901 can be run in either 12-hour or 24-hour mode. Byte 0Ah Bit 5 (HF) is defined as the 12- or 24-hour mode-select bit.

When the bit is 0, the 12-hour mode is selected. In the 12-hour mode, Byte 04h bit 7 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours).

Please note that all hour's values, including the alarms, must be re-entered whenever the 12/24-hour mode bit (HF) is changed.

Alarms

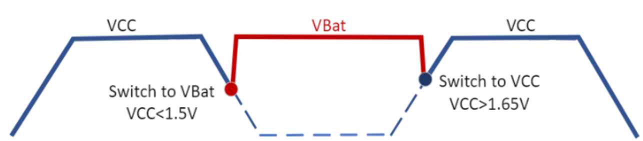
The SiT95901 supports time of day/date alarms. Alarm register can be set by writing to registers.

The alarms control can be enabled (using the Alarm Enable bit (AIE) in the Control Register) to activate the ALRT# on an alarm match condition.

V_{BAT}

The SiT95901 supports a low-power operation 32.768kHz RTC clock and calendar time keeping with only a coin cell battery supply. The coin cell battery power capacitance is usually 170 mAhr or higher, with less than 1 μA* low-power operation mode will maintain application system's date/time information up to few years.

The SiT95901 will switch V_{CC} to V_{BAT} for internal circuit when VCC is less than 1.5 V, I^{2}C will be off during the V_{BAT} operation time,



V_{CC}	V_{BAT}	Power Source
<1.5V	-	Vbat
>1.65V	-	VCC

Figure 4. V_{CC}/V_{BAT} Switch Timing

I^{2}C Mode Operations

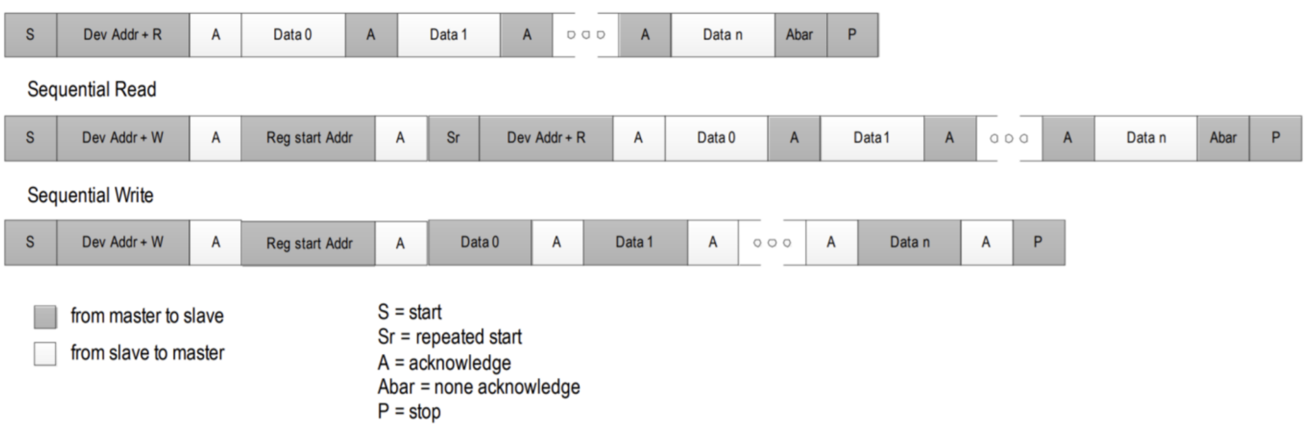
The SiT95901 RTC acts as a dual I^{2}C bus slave device using 7-bit 0x6F (8-bit 0xDE/DF) I^{2}C addresses to access RTC registers and allow two master devices connected in the server or other system. Similarly, the SiT95901 accesses SRAM using 7-bit 0x57 (8-bit 0xAE/AF) I^{2}C addresses.

The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data received in the byte write will be written immediately. For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Timeout: Timeout is where a slave device resets its interface whenever SCL or SDA goes low for longer than the timeout, which is in the range of 25mSec ~ 35mSec. This added logic deals with slave errors and recovering from those errors. When timeout occurs, the slave interface should re-initialize itself and be ready to receive a communication from the master, but it will expect a Start prior to any new communication.



Depending upon the state of the R/W bit, two types of data transfer are possible:

1) Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes.

The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The SiT95901 can operate in the following two modes:

1) Slave Receiver Mode (Write Mode):

Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see the "Data Write–Slave Receiver Mode" figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit SiT95901 address, which is 11011110, followed by the direction bit (R/W), which is 0 for a write.

After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. After the SiT95901 acknowledges the slave address + write bit, the master transmits a register address to the SiT95901. This sets the register pointer on the SiT95901, with the SiT95901 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the SiT95901 acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) Slave Transmitter Mode (Read Mode):

The first byte is received and handled as in the slave receiver mode.

However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the SiT95901 while the serial clock is input on SCL.

START and STOP conditions are recognized as the beginning and end of a serial transfer (see the "Data

Read–Slave Transmitter Mode" figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit SiT95901 address, which is 11011111, followed by the direction bit (R/W), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The SiT95901 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to

before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The SiT95901 must receive a "not acknowledge" to end a read.

Register map

Table 3. Register Specification

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Range	Binary Mode	Default	Primary I²C	Secondary I²C Access	Notes
00h	Seconds	0	b[6:4] x10 seconds			b[3:0] x1 seconds				00-59	00-3B	00	RW	RW	
01h	Second Alarm	0	b[6:4] x10 seconds			b[3:0] x1 seconds				00-59	00-3B	00	RW	RO	
02h	Minutes	0	b[6:4] x10 minutes			b[3:0] x1 minutes				00-59	00-3B	00	RW	RW	
03h	Minutes Alarm	0	b[6:4] x10 minutes			b[3:0] x1 minutes				00-59	00-3B	00	RW	RO	
04h	Hours (12H mode)	PM /AM	0	x10 hours		b[3:0] x1 hour				1-12	01-0C(AM) 81-8C(PM)	12	RW	RW	12-hour mode
	Hours (24H mode)	0	0	x10 hours		b[3:0] x1 hour				00-23	00-17		RW	RW	24-hour mode
05h	Hour Alarm (12H mode)	PM /AM	0	x10 hours		b[3:0] x1 hour				1-12	01-0C(AM) 81-8C(PM)	12	RW	RO	C0-FF: Don't Care
	Hour Alarm (24H mode)	0	0	b[5:4] x10 hours		b[3:0] x1 hour				00-23	00-17		RW	RO	C0-FF: Don't Care
06h	Day of the week	0	0	0	0	0	b[2:0] x1 Day of the week			01-07	01-07	07	RW	RW	Sunday=1, Default date: 2000,1,1
07h	Day of Month	0	0	b[5:0] x1 Day of the month						01-31	01-1F	01	RW	RW	
08h	Month	0	0	0	0	b[4:0] x1 Month				01-12	01-0C	01	RW	RW	
09h	Year	b[7:0] x1 year								00-99	00-63	00	RW	RW	
0Ah	Control register	ST	DM	HF	DSM	AIE	OFIE	CIE	TWO			00	RW	RO	
0Bh	Status register	AF	OF	RTC F	CIF	Rsvd	BVL2	BVL1	BVL0				RW	RO	
0Ch	CLKOUT control	CKE	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	b[1:0] CKD				00	RO	RW	Enable write from the secondary I²C for CLKOUT control to support clock calibration
0Dh	Secondary control register	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	MWO			00	RW	RO	Additional control registers
0Eh	Scratchpad	Scratchpad register										00	RW	RO	
0Fh	Version ID	b[7:4] Major version				b[3:0] Minor version						10	RO	RO	0x10: match the first version
10h	Vendor ID	b[7:0] Vedor ID Code										03	RO	RO	Vendor ID information,
11h	Model	Model code											RO	RO	
12h-1D	Reserved	Reserved											Rsvd	Rsvd	
1Eh	VBAT_DET _CTRL	Rsvd	ADC_E N_SEL	ADC_E N	VBAT_ DET_R EQ	VBAT_ DET_C LK_SEL	VBAT_D ET_TIME					2D	RW	RO	Bit[4] is RW for primary/secondary
1Fh-FFh	Reserved	Reserved											Rsvd	Rsvd	

Table 4. Register bit Specification

Bit	Function
Stop (ST)	1: Stop the Real-Time Clock (RTC) 0: Normal mode The function of the stop (ST) bit is to allow for accurate starting of the time circuits, the ST bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the 1.024Hz, 32 Hz, and 1 Hz clocks.
Data Mode (DM)	1: Binary mode 0: Binary-Coded Decimal (BCD) mode
Hour Format (HF)	1: 24-hour mode 0: 12-hour mode
Daylight-Saving Mode (DSM)	1 Enable the DSM 0: Disable the DSM ▪ The first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. ▪ The last Sunday in October when the time first reaches 1:59:59 AM, it is backward to 1:00:00 AM
Alarm Interrupt Enable (AIE)	1: Enable the alarm interrupt. Allows an interrupt to occur when the Alarm Flag (AF) is set from an alarm match from the update cycle. 0: Disable the alarm interrupt
Oscillator Fail Interrupt Enable (OFIE)	1: Enable the oscillator fail interrupt 0: Disable the oscillator fail interrupt
RTC Clear Interrupt Enable (CIE)	1: Enable the interrupt (ALRT# assertion) when the RTC_CLR# assertion is detected 0: Disable the interrupt
Time-Register Write Ownership (TWO)	0: The secondary I^2C* has write access to the time registers 1: The primary I^2C* has write access to the time registers Note: This bit is only writeable from the primary I^2C*
RTC_Clear Flag (CIF)	Set when the RTC_CLR# pin assertion is detected. Write 0 to clear
Alarm Flag (AF)	1: After all the alarm values match the current time. Write 0 to clear
RTC Power Fail Bit (RTCF)	1: Set when the device powers up after losing all power (Voltage Common Collector [VCC] and Battery Voltage [VBAT]). Write 0 to clear
Oscillator Fail (OF) Bit	1: The Oscillator Fail flag (OF) is set when the oscillator fails or stops. Write 0 to clear the flag set in the following conditions: ▪ First time power is applied. ▪ Oscillator has failed (the frequency is either zero or very far away from the desired 32.768 kHz) ▪ The Stop (ST) bit is set to 1
Clock Output Enable (CKE)	0: The CLKOUT output is inhibited, and the pin is set to high impedance 1: The clock output is activated Note: The clock output is always disabled when only powered by VBAT(VCC is not valid)
Clock Output Divisor (CKD)	00:32.768 kHz 01: 1.024 kHz 10: 32 Hz 11:1 HZ
SRAM Write Ownership (MWO)	0: The secondary I^2C* has write access to the SRAM registers 1: The primary I^2C* has write access to the SRAM registers Note: This bit is only writeable from the primary I^2C*
Battery Voltage Level (BVL) [2:0]	000: BVL <=1.7V 001: BVL [1.7V 1.9V] 010: BVL [1.9V, 2.1V] 011: BVL [2.1V, 2.3V] 100: BVL [2.3V, 2.5V] 101: BVL [2.5V, 2.7V] 110: BVL [2.7V, 3.0V] 111: BVL > 3.0V

Table 5. Detailed Register Map Description

Block	Register Address
RTC Register	I^2C slave address: 7-bit 0x6F 0x00~0x11: User Registers 0x11~0xFF: Vendor Registers
SRAM	I^2C slave address: 7-bit 0x57 0x00~0x7F: 128-byte battery-backed SRAM

User Registers

Second Register (SECOND)

Address: 0x00

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	RSV	0	RO	RO	Reserved
6:4	SEC_HIGH	0	RW	RW	Value in X10 seconds. In BCD (Binary-Coded Decimal Data) Mode, [6:0] range is 00~59; in Binary Mode, [6:0] range is 0x00~0x3B. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.
3:0	SEC_LOW	0	RW	RW	Value in X1 seconds. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Second Alarm Register (SECOND_ALARM)

Address: 0x01

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	RSV	0	RO	RO	Reserved
6:4	SEC_ ALARM_ HIGH	0	RW	RO	Value in X10 seconds. In BCD (Binary-Coded Decimal Data) Mode, [6:0] range is 00~59; in Binary Mode, [6:0] range is 0x00~0x3B. 0xC0~0xFF indicates “Don’t care” situation.
3:0	SEC_ ALARM_ LOW	0	RW	RO	Value in X1 seconds

Minute Register (MINUTE)

Address: 0x02

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	RSV	0	RO	RO	Reserved
6:4	MIN_HIGH	0	RW	RW	Value in X10 minutes. In BCD (Binary-Coded Decimal Data) Mode, [6:0] range is 00~59; in Binary Mode, [6:0] range is 0x00~0x3B. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.
3:0	MIN_LOW	0	RW	RW	Value in X1 minutes. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Minute Alarm Register (MINUTE_ALARM)

Address: 0x03

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	RSV	0	RO	RO	Reserved
6:4	MIN_ ALARM_ HIGH	0	RW	RO	Value in X10 minutes. In BCD (Binary-Coded Decimal Data) Mode, [6:0] range is 00~59; in Binary Mode, [6:0] range is 0x00~0x3B. 0xC0~0xFF indicates “Don’t care” situation.
3:0	MIN_ ALARM_ LOW	0	RW	RO	Value in X1 minutes

Hour Register (HOUR)

Address: 0x04

12-hour mode (HF bit Register Control is “0”)

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	PM_AMn	0	RW	RW	PM or AM flag. 0=AM, 1=PM
6	RSV	0	RW	RW	Reserved
5:4	HOUR_ HIGH	1	RW	RW	Value in X10 hours. In BCD (Binary-Coded Decimal Data) Mode, [5:0] range is 01~12; in Binary Mode, [5:0] range is 0x01~0x0C. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.
3:0	HOUR_ LOW	2	RW	RW	Value in X1 hours. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

24-hour mode (HF bit Register Control is “1”)

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:6	RSV	0	RW	RW	Reserved
5:4	HOUR_ HIGH	0	RW	RW	Value in X10 hours. In BCD (Binary-Coded Decimal Data) Mode, [5:0] range is 00~23; in Binary Mode, [5:0] range is 0x00~0x17. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.
3:0	HOUR_ LOW	0	RW	RW	Value in X1 hours. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Hour Alarm Register (HOUR_ALARM)

Address: 0x05

12-hour mode (HF bit Register Control is “0”)

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	PM_AMn	0	RW	RO	PM or AM flag. 0=AM, 1=PM
6	RSV	0	RW	RO	Reserved
5:4	HOUR_ ALARM_ HIGH	1	RW	RO	Value in X10 hours. In BCD (Binary-Coded Decimal Data) Mode, [5:0] range is 01~12; in Binary Mode, [5:0] range is 0x01~0x0C. 0xC0~0xFF indicates “Don’t care” situation.
3:0	HOUR_ ALARM_ LOW	2	RW	RO	Value in X1 hours.

24-hour mode (HF bit Register Control is “1”)

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:6	RSV	0	RW	RO	Reserved
5:4	HOUR_ ALARM_ HIGH	0	RW	RO	Value in X10 hours. In BCD (Binary-Coded Decimal Data) Mode, [5:0] range is 00~23; in Binary Mode, [5:0] range is 0x00~0x17. 0xC0~0xFF indicates “Don’t care” situation.
3:0	HOUR_ ALARM_ LOW	0	RW	RO	Value in X1 hours.

Day Register (DAY)

Address: 0x06

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	DAY	0x7	RW	RW	Day of the week. In BCD/Binary Mode, range is 1~7. 1= Sunday, 2=Monday, 3=Tuesday, 4=Wednesday, 5=Thursday, 6=Friday, 7=Saturday Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Date Register (DATE)

Address: 0x07

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	DATE	0x01	RW	RW	Date of the month. In BCD mode, range is 1~31; in Binary mode, range is 0x01~0x1F. Write access ownership controlled by Time-Register Write Ownership (TWO) bit. The device simply assumes that all the years divisible by four are leap years in which the 29th day is added in February.

Month Register (MONTH)

Address: 0x08

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	MONTH	0x01	RW	RW	Month. In BCD mode, range is 1~12; in Binary mode, range is 0x01~0x0C. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Year Register (YEAR)

Address: 0x09

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	YEAR	0x00	RW	RW	Year. In BCD mode, range is 0~99; in Binary mode, range is 0x00~0x63. Write access ownership controlled by Time-Register Write Ownership (TWO) bit.

Control Register (CONTROL)

Address: 0x0A

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	ST	0x0	RW	RO	Stop time. 0= Normal mode 1= Stop the Real-Time Clock (RTC)
6	DM	0x0	RW	RO	Data mode selection. 0= Binary-coded Decimal (BCD) mode 1= Binary mode
5	HF	0x0	RW	RO	Hour format selection 0= 12-hour mode 1= 24-hour mode
4	DSM	0x0	RW	RO	Daylight-Saving mode selection 0= Disable the DSM 1= Enable the DSM Daylight Saving specification: First Sunday in April: time increments from 1:59:59 am to 3:00:00 am Last Sunday in October, time changes back to 1:00:00 am from first 1:59:59 am
3	AIE	0x0	RW	RO	Alarm interrupt enable 0= Disable the alarm interrupt 1= Enable the alarm interrupt. Allows an interrupt to occur when the Alarm Flag (AF) is set from an alarm match from the update cycle Reset by RTC_CLR#.
2	OFIE	0x0	RW	RO	Oscillator fail interrupt enable 0= Disable the oscillator fail interrupt 1= Enable the oscillator fail interrupt Reset by RTC_CLR#.
1	CIE	0x0	RW	RO	RTC clear interrupt enable 0= Disable RTC clear interrupt 1= Enable RTC clear interrupt
0	TWO	0x0	RW	RO	Time-register write ownership 0= 2nd I2C has write access to the time registers (Reg 0x00, 0x02, 0x4, 0x6, 0x7, 0x8, 0x9) 1= 1st I2C has write access to the time registers

Status Register (STATUS)

Address: 0x0B

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	AF	0x0	RW	RO	Alarm flag, set when all the alarm values match the current time, cleared by writing “0”. Reset by RTC_CLR#
6	OF	0x1	RW	RO	Oscillator fail flag, cleared by writing “0”, set by the following conditions: Fist time power is applied. Oscillator has failed (the frequency is either zero or very far away from the desired 32.768KHz) The Stop (ST) bit is set to “1”
5	RTCF	0x1	RW	RO	RTC power fail flag, set when the device powers up after losing all power (VCC voltage & battery voltage), cleared by writing “0”
4	CIF	0x0	RW	RO	RTC clear assertion flag, set when RTC_CLR# pin assertion is detected, cleared by writing “0”
3	RSV	0x0	RO	RO	Reserved
2:0	BVL	0x0	RO	RO	Battery voltage level 0x0= <= 1.7V 0x1= 1.7V~1.9V 0x2= 1.9V~2.1V 0x3= 2.1V~2.3V 0x4= 2.3V~2.5V 0x5= 2.5V~2.7V 0x6= 2.7V~3.0V 0x7= > 3.0V

Clkout Control Register (CLKOUT_CTRL)

Address: 0x0C

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	CKE	0x0	RO	RW	Clock output enable. 0= CLKOUT output is inhibited, and the pin is set to high-impedance 1= Enable CLKOUT output
6:2	RSV	0x0	RO	RO	Reserved
1:0	CKD	0x0	RO	RW	Select CLKOUT frequency. 0x0= 32.768 KHz 0x1= 1.024 KHz 0x2= 32 Hz 0x3= 1Hz

Second Control Register (CONTROL2)

Address: 0x0D

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:1	RSV	0x0	RO	RO	Reserved
0	MWO	0x0	RW	RO	SRAM write ownership 0= 2nd I2C has write access to SRAM registers 1= 1st I2C has write access to SRAM registers Reset by RTC_CLR#

Scratchpad Register (SCRATCH)

Address: 0x0E

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	DATA	0x0	RW	RO	Scratch pad data

Version Register (VERSION)

Address: 0x0F

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:4	MAJ_VER	0x1	RO	RO	Major version. [7:0] = 0x10 indicating the first version 0x1= First version
3:0	MIN_VER	0x0	RO	RO	Minor version

Vendor ID Register (SCRATCH)

Address: 0x10

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	VEND_ID	0x03	RO	RO	Vendor identifier

Model Register (MODEL)

Address: 0x11

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7:0	MOD_CODE	N/A	RO	RO	Model code 0x00 = Rev A0 0x01 = Rev A1 0x01

Battery Voltage Detection Control Register (VBAT_DET_CTRL)

Address: 0x1E

BIT	FIELD	DEFAULT	Primary I²C	Secondary I²C	Description
7	RSV	0	RO	RO	Reserved
6	ADC_EN_SEL	0	RW	RO	Some ADC block auto-power on 0x0= the ADC block is enabled during ADC conversion. 0x1= the ADC block is controlled by ADC_EN
5	ADC_EN	1	RW	RO	Enable ADC
4	VBAT_DET_REQ	0	RW	RO	Manually request to detect battery voltage. Trigger battery voltage detection by writing “1” into this bit. This bit will be self-cleared when the battery voltage detection is finished.
3:2	VBAT_DET_CLK_SEL	0x3	RW	RO	Select battery voltage detection clock. 0x0= divided-by-2 clock of system clock 0x1= divided-by-4 clock of system clock 0x2= divided-by-6 clock of system clock 0x3= divided-by-8 clock of system clock
1:0	VBAT_DET_TIME	0x1	RW	RO	Battery voltage detection time control 0x0= No automatically battery voltage detection 0x1= Do battery voltage detection daily 0x2= Do battery voltage detection weekly 0x3= Do battery voltage detection monthly

Electrical Characteristics

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Max	Unit
Supply voltage	V_{CC}		+3.6	V
Supply current	I_{CC}		±1	mA
Battery supply voltage	V_{BAT}		+3.6	V
Battery supply current	I_{BAT}		±10	µA
Input voltage	VI	SCL, SDA, OSCI, RTC_CLR#	+3.6	V
Output voltage	VO		+3.6	V
Input current	I_{IN}	At any input	+10	mA
Output current	I_{OUT}	At any input	+10	mA
Total power dissipation	P_{tot}		3.6	mW
Electrostatic discharge	ESD	HBM	±2000	V
		CDM	±1000	V
Latch-up current	I_{LU}		±200	mA
Storage temperature	T_{STG}		+150	˚C

Table 7. Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}		1.7		3.6	V
Battery supply voltage	V_{BAT}		1.55		3.6	V
Timekeeping battery current	I_{BAT}	@25°C, Vbat=3.3 V, CLKOut OFF Average value over 1S		0.6	1.0	µA
Timekeeping battery current		@-40C...+85°C, Vbat=3.3 V, CLKOut OFF		0.7	1.5	µA
Peak battery current		Maximum instant peak current on Vbat pin			1	mA
Supply current	I_{CC}	@25°C, full active mode CLKOUT at 32.768K with VCC = 1.8 V			1	mA
Switchover from Vcc to battery (Vcc falling)	Vsw_1	Start to switch to battery when Vcc is less than 1.5 V	1.4	1.45	1.5	V
Switchover from battery to Vcc (Vcc rising)	Vsw_2	Switch back to Vcc when Vcc voltage is higher than 1.65 V	1.55	1.6	1.65	V
Input voltage	V_I		-0.5		+3.6	V
Low-level input voltage	V_{IL}		-	-	0.3 x V_{CC}	V
High-level input voltage	V_{IH}		0.7 x V_{CC}	-	-	V
Input leakage current	I_{LI}		-1	-	+1	µA
RTC_CLR# input high voltage	RTC_CLR# V_{IH}		1.2		3.6	V
RTC_CLR# input low voltage	RTC_CLR# V_{IL}		-0.3		+0.5	V
RTC_CLR# minimum insertion period	RTC_CLR# Tmin				32	µs
Input capacitance	C_{IN}		-	1	-	pF
High-level output voltage	V_{OH}	CLKOUT pin	0.8 x V_{CC}	-	V_{CC}	V
Low-level output voltage	V_{OL}		0	-	0.2 x V_{CC}	
High-level output current	I_{OH}	V_{OH} = 2.9 V, VDD = 3.3 V, on pin CLKOUT	1	3	-	mA
Low-level output current	I_{OL}	Output sink current (Vol=0.4 V), VCC=3.3 V, SDA, ALERT# pins	3	8.5	-	mA
		Output sink current (Vol=0.4 V), VDD=3.3 V, CLKOUT Pins	1	4	-	mA

Table 8. Recommended Operating Temperature and Thermal Characteristics

Description	Symbol	Min	Typ	Max	Unit
Storage Temperature		-55		+125	°C
Soldering Temperature				+260	°C
Ambient Operating Temperature	TA	-40		+85	°C

Table 9. Crystal Specification

Description	Conditions	Symbol	Min	Typ	Max	Unit
Crystal Frequency	Nominal Frequency	$XTAL_{IN}$		32.768		kHz
Crystal frequency accuracy	Nominal accuracy		-23		+23	ppm
	Accuracy cross temperature (0...+40°C) and voltage		-46		+46	ppm
CL cap for crystal	Load Capacitance	$XTAL_{CL}$		12.5		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$			50	kΩ
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW

Notes:

1. ESR relates to the motional resistance Rm with the relationship $ESR = Rm\ (1 + C0/CL)^2$

I^{2}C interface

Single Byte Write

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit data to be written to the register map address specified
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition

Single Byte Read

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition
- The master re-initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 1 (read)
- The slave then writes the 8-bit data to be written to the register map address specified
- The master does not acknowledge this transaction as the slave may assume a multi-byte read operation and there is a risk of slave holding the bus low
- The master ends the transaction by issuing a stop condition

Multi Byte Read

The multi-byte read mode is used to read a continuous segment of the register map. The multi-byte read is faster than performing multiple single byte reads as the device address and register map address need not be specified for every byte read from the register map

The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)

- The slave acknowledges by driving zero on the bus
- The master then writes the 8 bit register map address
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition
- The master re-initiates the transaction by issuing a start condition, writes 7 bit slave address and then the read/write bit is written as 1 (read)
- The slave then writes the 8 bit data to be written to the register map address specified
- The master acknowledges by driving zero on the bus
- The slave automatically increments the register map address and writes the data in at that address to the bus and the master acknowledges
- When all bytes of data are read, master ends the operation by not acknowledging the last read
- The master then ends the transaction by issuing a stop condition

Read Operation - Single Byte

S	Slave Addr [6:0]	0	A	Reg Addr [7:0]	A	P

S	Slave Addr [6:0]	1	A	Data [7:0]	N	P

Read Operation - Burst (Auto Address Increment)

S	Slave Addr [6:0]	0	A	Reg Addr [7:0]	A	P

S	Slave Addr [6:0]	1	A	Data [7:0]	A	$\underbrace{\text{Data [7:0]}}_{\text{Reg Addr + 1}}$	N	P

Host ← AU1901

Host → AU1901

1- Read, 0 - Write, A - Acknowledge, N - Not Acknowledge, S - Start Condition, P - Stop Condition

Write Operation - Single Byte

S	Slave Addr [6:0]	0	A	Reg Addr [7:0]	A	Data [7:0]	A	P

Host ← AU1901

Host → AU1901

1- Read, 0 - Write, A – Acknowledge (SDA LOW), N - Not Acknowledge (SDA HIGH), S - Start Condition, P - Stop Condition

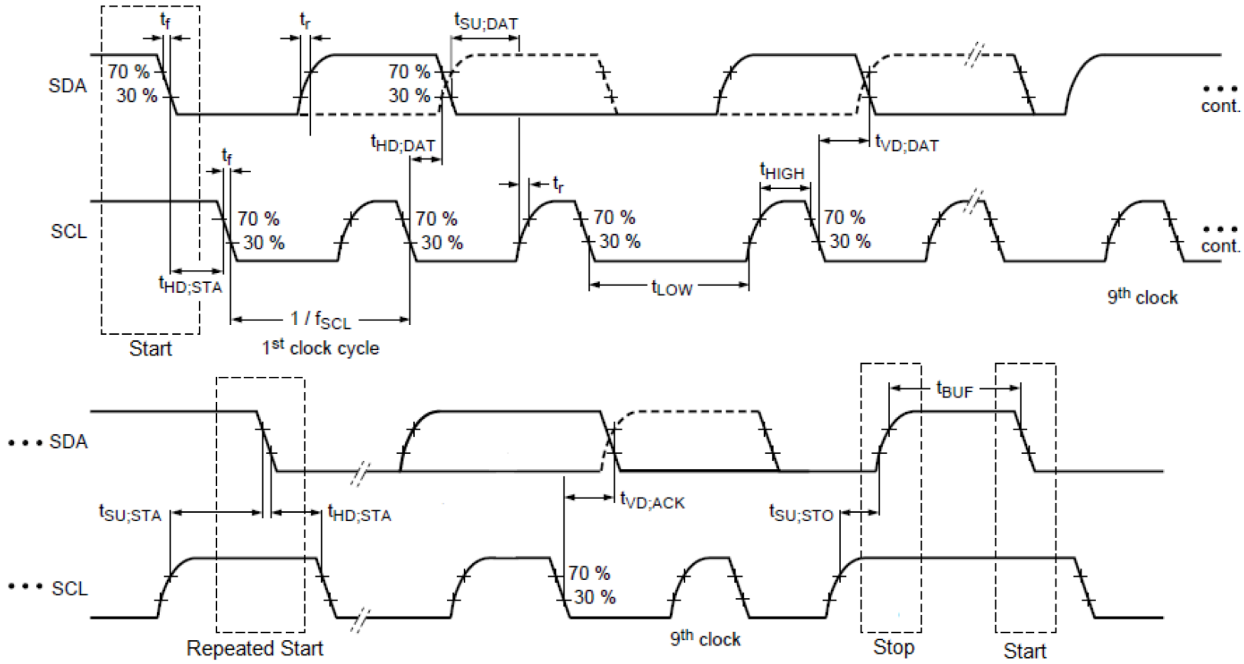


Figure 5. I²C Timing Waveform

Table 10. I²C Bus timing specifications

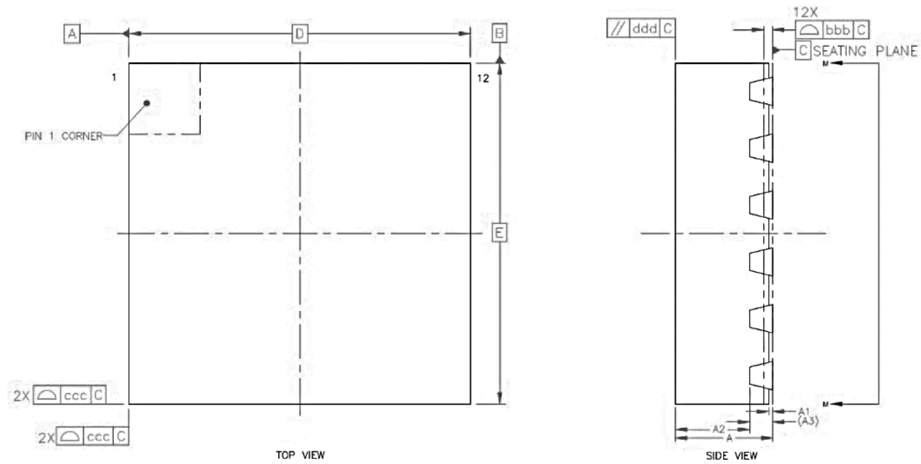
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C Timeout	t_{TO_SCL}	Detect I²C clock low timeout	25		35	ms
	t_{TO_SDA}	Detect I²C data low timeout	25		35	ms
Serial Clock Frequency	f_{SCLK}			100	400	kHz
Bus free time between STOP and START	t_{BUF}		1.3			µs
START Setup time	$t_{SU:STA}$		0.6			µs
START Hold time	$t_{HD:STA}$		0.6			µs
SDA signal Setup time	$t_{SU:DAT}$		100			ns
SDA signal Hold time[2]	$t_{HD:DAT}$		0			µs
Rise time for SDA/SCLK	t_r				300	ns
Fall time for SDA/SCLK	t_f				300	ns
SCLK High time	t_{HIGH}		0.6			µs
SCLK Low time	t_{LOW}		1.3			µs
STOP setup time	$t_{SU:STO}$		0.6			µs
Capacitive load for pins	C_B	SDA or SCLK			400	pF
Data valid time	$T_{VD:DAT}$				0.9	µs
Data valid acknowledge time	$T_{VD:ACK}$					
Glitch filter	T_{SP}				50	ns

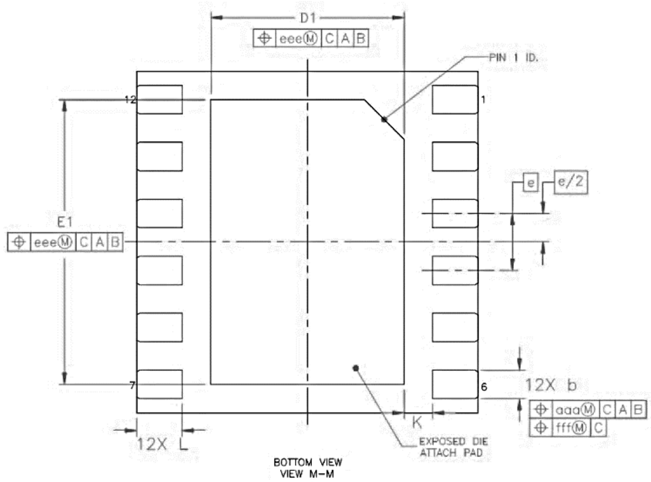
Notes:

2. These specifications are guaranteed by design and not tested in production.
3. The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms.
4. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)





PACKAGE TYPE		SON[DFN]		
PIN COUNT		12		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	–	0.65	0.67
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	2.90	3.0	3.10
	E	2.90	3.0	3.10
EP SIZE	D1	1.60	1.70	1.80
	E1	2.40	2.50	2.60
LEAD LENGTH	L	0.35	0.40	0.45
LEAD PITCH	e	0.5 BSC		
LEAD WIDTH	b	0.20	0.25	0.30
LEAD POSITION OFFSET	aaa	0.10		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.15		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		
EXP PAD TO LEAD EDGE	K	0.15	0.25	0.35

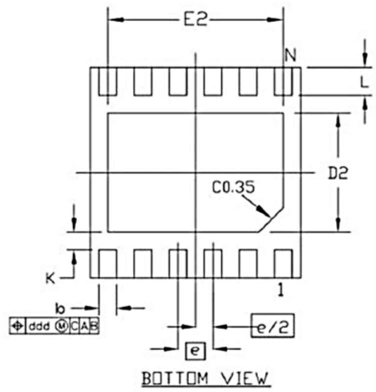
NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

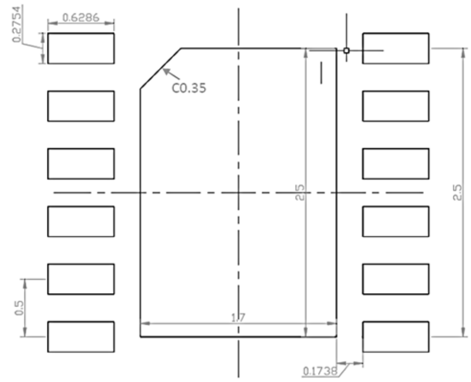
2.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMNAL TIP.

Recommended Land Pattern (Unit: mm)

Package foot print(Device)



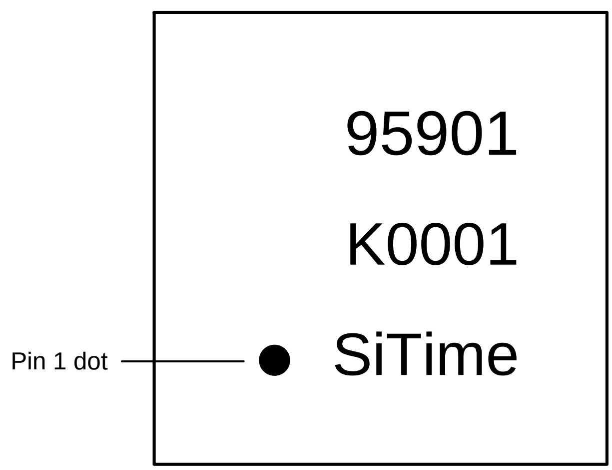
PCB Land Pattern dimension(Recommend)



TOP View

Notes:
1. All dimensions in millimeters.
2. All dimensions tolerance should follow ANSI Y14.5M-1994 spec.
3. NSMD Preferred.

Top Marking

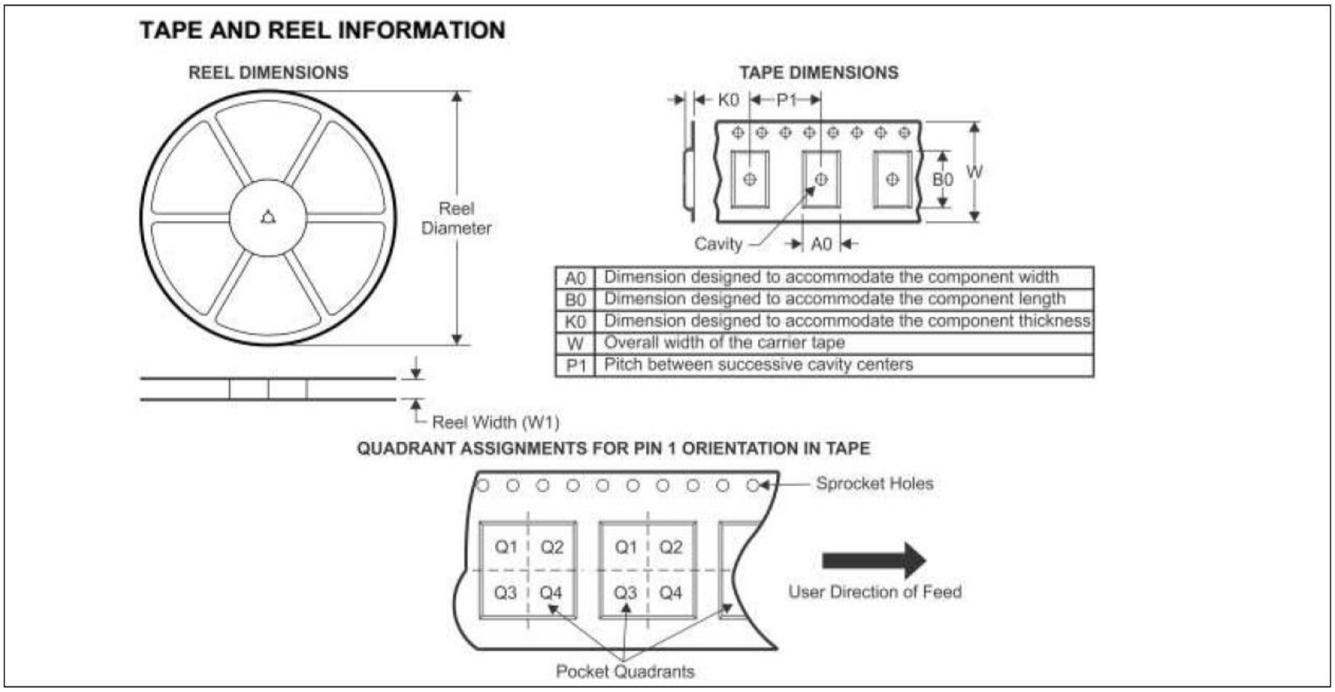


Line 1: 95901, SiTime part#

Line 2: “xxxxx”, Lot# code from SiTime, example: K0001

Line 3: Pin 1 dot and “SiTime” logo

Tape and Reel information



Product	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SiT95901	DFN 3x3	12	4000	330	12.4	3.3	3.3	1.1	8	12	Q1

Figure 6. Tape and Reel information

Revision History

Table 11. Revision History

Version	Release Date	Change Summary
1.0	13-Feb-2024	Initial Release
0.11	13-Jun-2024	Updated device top marking section
0.12	4-Mar-2025	Updated with “P” Tape and Reel packaging code

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