Description

The SiT92318 family of parts are HCSL Low-Power (HCSL-LP), 8 output differential Fan-Out buffers that meet or exceed all the performance requirements of the Intel DB800Z specification. They are suitable for PCI Express Gen.1–6 or QPI/UPI applications.

The SMBus interface and multiple output-enable pins allow the configuration and control of all 8 outputs individually.

It is packaged in a compact VQFN package and uses a standard pin configuration.

Applications

- Micro server and Tower Server
- Rack server
- Storage area network and host bus adapter card
- Network attached storage
- Hardware accelerator

Features

- HCSL-LP outputs with Zo = 85 Ω
- Saves power and board space - no termination resistors required
- Supports PCIe and QPI applications
- Spread spectrum compatible; tracks spreading input clock for low EMI
- Additive phase jitter
- Fclk=100 MHz (10k-20M) band ~ 50fs (typical)
- Fclk=100 MHz after PCIE Gen5 (CC) filter ~12 fs RMS
- Fclk=100 MHz after PCIE Gen6 filter ~8 fs RMS
- Additive phase jitter after DB800Z filter ~10 fs RMS (typical)
- Programmable output slew rate control
- 3.3 V core and IO supply voltages
- Hardware-controlled low power mode (PDN)
- Current consumption: 62 mA Typical with all 8 outputs enabled at 100 MHz, driving a 10 inch T line and 2 pF load on each output

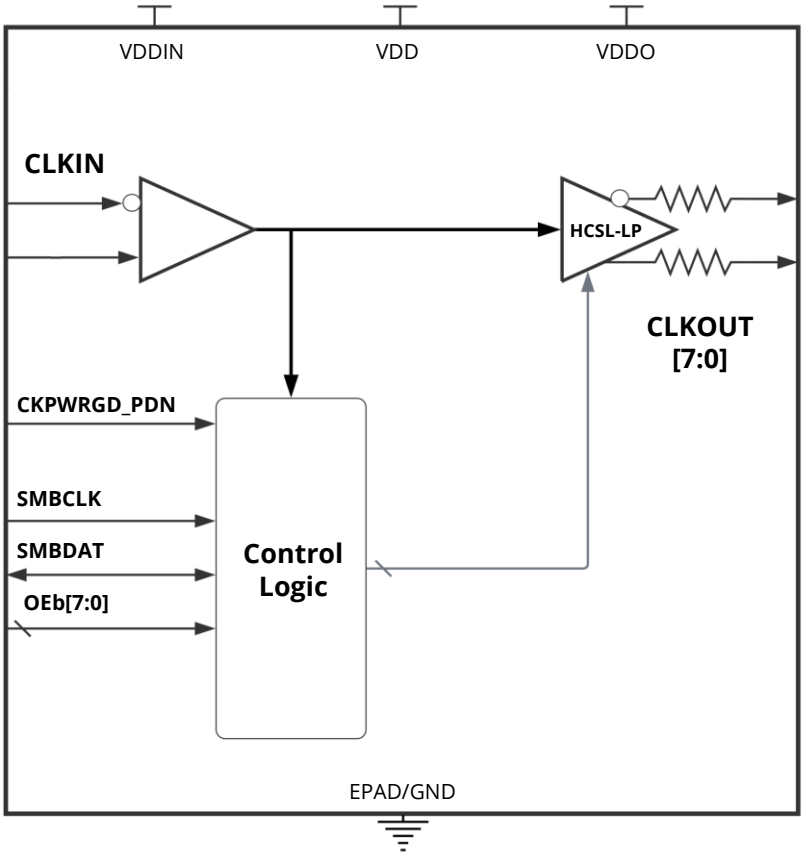

Figure 1. SiT92318 Functional Overview

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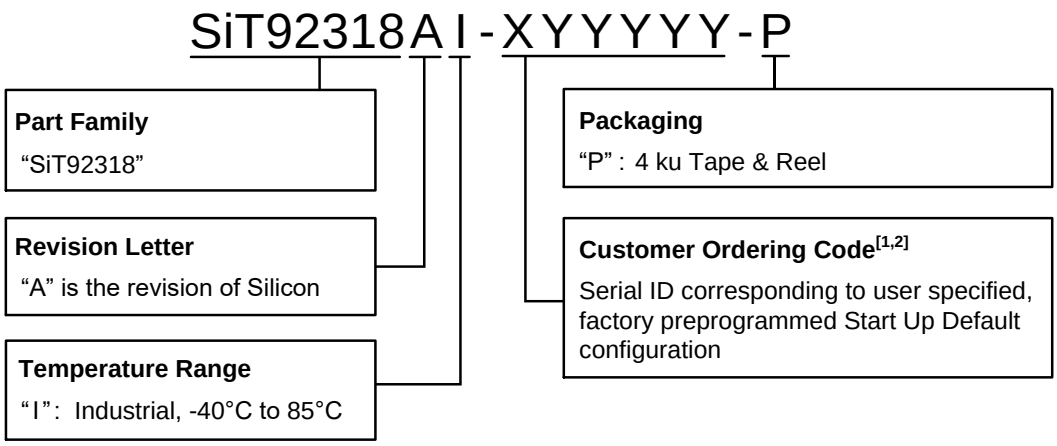
Ordering Information



Notes:

1. X = "A" and "B" customer device, "C" to "Z" reserved.
   a. A:Denotes blank devices;
   b. B: Denotes Pre-configured devices, contact SiTime for the specifics
2. Y = 0..9, A…Z for custom serial ID.

Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage	Input Supply Core Supply	VDDIN VDD			**3.63**	V
Output Bank Supply Voltage	Output Driver Supply	VDDO			**3.63**	V
Input Low Voltage		V_{IL}	GND-0.5			V
Input High Voltage	Except for SMBus interface	V_{IH}			VDD+0.5	V
Input High Voltage	SMBus clock and data pins	V_{IHSMB}			3.6	V
Storage Temperature		Ts	-65		150	°C
Junction Temperature		Tj			125	°C
ESD (Human Body Model)	JESD22A-114	ESDHBM			2000	V
ESD(Charge Device Model)		ESDCDM			500	V
Latch Up	JEDEC JESD78D	LU			100	mA
Moisture Sensitivity Level		MSL	3			

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Supply and Temperature

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Supply Voltage		VDDIN	2.97	3.3	3.465	V
Core Supply Voltage		VDD	2.97	3.3	3.465	V
Output Supply Voltage		VDDO	2.97	3.3	3.465	V
Ambient Temperature		T_A	-40		85	°C
Junction Temperature		T_j			125	°C

Table 3. Electrical Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Supply Current	Input Supply Current	IDD_{VDDIN}		6.6		mA
	Core Supply Current	IDD_{VDD}		8		mA
Additive Output Supply Current	All Outputs Enabled, driving a 10in T-line terminated with 2 pF cap at 100 MHz clock	IDD_{VDDO}		48		mA
Power Down Current	CKPWRGD = 0	IDD_{VDDIN}		1		mA
		IDD_{VDD}		4.5		mA
		IDD_{VDDO}		5.3		mA
Power Down Current, Low Power Mode	CKPWRGD = 0, with SMBUS control	IDD_{VDDIN1}		0.1		mA
		IDD_{VDD1}		3		mA
		IDD_{VDDO1}		0.1		mA
Input Control Pin Characteristics						
Input High Current	VDDIN = 3.3 V, VIH = VDDIN	I_{IH}			20	µA
Input Low Current		I_{IL}	-0.5			µA
Input high voltage – Logic inputs		V_{IH}	0.7xVDDIN			V
Input low voltage – Logic inputs		V_{IL}			0.3xVDDIN	V
Internal Pull-down resistance		$R_{Pulldown}$		200		KΩ
Pin Inductance		L_{PIN}			7	nH
Capacitance	Logic Inputs, except DIF_IN.	C_{IN}			4.5	pF
	DIF_IN differential clock inputs[2]	C_{INDIF_IN}			2.7	
	Output pin capacitance	C_{OUT}			4.5	

Notes:

1. All parameters are guaranteed by design and characterization, not tested in production.
2. DIF_IN input.

Table 4. Input Clock Characteristics

Unless otherwise specified: VDDIN = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin driven differentially.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input frequency range		F_{CLKin}	1		400M	Hz
Peak differential input voltage swing		VID	0.1			V
Input Slew Rate - CLK_{IN}	Measured differentially	dv/dt	0.2		4	V/ns
Input Leakage Current	VIN = VDD, VIN = GND	I_{IN}	-5		5	uA
Input Duty Cycle	Measurement from differential waveform	d_{TIN}		50		%
Input Crossover Voltage	Crossover voltage		0.1		0.9	V

Table 5. Output Clock Characteristics (HCSL-LP) at 100 MHz

$T_A = T_{COM}$; Supply Voltage VDDO = 3.3 V +/-5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Slew rate	Scope averaging on	T_{rf}	2		4	V/ns
Slew rate matching	Slew rate matching, Scope averaging on	ΔT_{rf}			20	%
Voltage High	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	V_{High}		750		mV
Voltage Low		V_{Low}		0		mV
Max Voltage	Measurement on single ended signal using absolute value. (Scope averaging off)	V_{max}				mV
Min Voltage		V_{min}				
Vswing	Scope averaging off	V_{SWING}				mV
Crossing Voltage (abs)	Scope averaging off	V_{cross_abs}		375		mV
Crossing Voltage (var)	Scope averaging off	Δ-Vcross				mV
Differential Impedance		Z_{DIFF}		85		Ω
Clock Stabilization[1,2]	From VDDO power-up and after input clock stabilization or de-assertion of PDb to 1st Clock	T_{STAB}		1.0	1.8	ms
OEb Latency[1,2,3]	DIF starts after OEb assertion DIF stop after OEb de-assertion	t_{LATOEb}	2		3	Clocks
Tdrive_PDb[1,3]	DIF output enable after PDb de-assertion	t_{DRVPDb}		76	300	µs
T_{FALL}[2]	Fall time of control inputs	t_F			5	ns
T_{RISE}[2]	Rise time of control inputs	t_R			5	ns
Output high voltage	Single ended, measured into DC test load	V_{OH}	225		270	mV
Output low voltage	Single ended, measured into DC test load	V_{OL}	10		120	mV
Over shoot voltage	Single ended, measured into DC test load	V_{OVS}			V_{OH}+75	mV
Under shoot voltage	Single ended, measured into DC test load	V_{UDS}			V_{OL}-75	mV
Differential Impedance[4]		Z_{DIFF}	85-5%	85	85+5%	Ω
Differential Impedance (crossing)[5]		Z_{DIFF_CROSS}	85-20%	85	85+20%	Ω

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing.
3. Time from deassertion until outputs are > 200mV.
4. Measured at V_{OH}/V_{OL}
5. Measured at transition.

Table 6. SMbus Electrical Parameters

$T_A = T_{AMB}$. Supply voltages are per normal conditions. See Test loads for loading conditions.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SMBus Input Low Voltage		V_{ILSMB}			0.8	V
SMBus Input High Voltage		V_{IHSMB}	2.1		VDD_{SMB}	V
SMBus Output Low Voltage	At I_{PULLUP}	V_{OLSMB}			0.4	V
SMBus Sink Current	At V_{OL}	I_{PULLUP}	4			mA
Nominal Bus Voltage		VDD_{SMB}	2.7		3.6	V

Table 7. Skew and Differential Jitter Parameters

Parameter	Conditions	Symbol	Min	Typ	Max	Units
CLK INx, CLKOUTx[1,2,4,5,6,7]	Input-to-Output Skew in nominal value @ 25°C, 3.3 V	t_{PD}		0.75		ns
CLKINx, CLKOUTx [1,2,6,7,8]	Input-to-Output Skew Variation across temperature	T_{PD_DRIFT}				ps
DIF[2,5,6,7]	Output-to-Output Skew across all outputs	t_{SKEW_ALL}			50	ps
Duty Cycle Distortion[3,5,6]	Measured differentially, @100MHz	t_{DCD}				%

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Differential cross-point to differential cross-point measurement.
3. The difference in Duty Cycle between the output and input clock is referred as Duty Cycle Distortion
4. Mean Value measured through scope averaging.
5. Measured from differential waveform.
6. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
7. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
8. This is the amount of input-to-output delay variation with respect to temperature.

Table 8. Phase Jitter Parameters-PCIe Common Clocked (CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1 HF [1,2,3,4]	$tjph_{PCIeG1-CC}$		0.100		ps (p-p)
	PCIe Gen 2 HF [1,2,3,4]	$tjph_{PCIeG2-CC}$		0.080		ps rms
	PCIe Gen 3[1,2,4]	$tjph_{PCIeG3-CC}$		0.023		ps rms
	PCIe Gen4[1,2,4]	$tjph_{PCIeG4-CC}$		0.023		ps rms
	PCIe Gen5[1,2,4]	$tjph_{PCIeG5-CC}$		0.009		ps rms
	PCIe Gen6[1,2,4]	$tjph_{PCIeG6-CC}$		0.006		ps rms

Notes:

1. Guaranteed by design and characterization. Applies to all differential outputs.
2. Input to SiT92318 is fed using low phase noise source SMA100B while SiT92318 is configured as 100 MHz LP-HCSL Output Driver and fed to the channels of the DSO through low noise high slew drivers to minimize the impact of DSO broadband noise.
3. Additive RMS Jitter Measurement for PCIe are made using DSO. Commercially available and popular PCIe jitter post processing tools are used to report PCIe jitter
4. Additive jitter for RMS values is calculated by solving the equation for b [$b = \sqrt{(c^2 - a^2)}$] where 'a' is the rms input jitter and "c" is the rms total jitter.
5. Input to SiT92318 is fed using low phase noise source SMA100B, SiT92318 is configured as 100MHz HCSL Output Driver [VDDOx = 3.3 V] and fed to the channels of DSA90804A using the exact measurement set up.

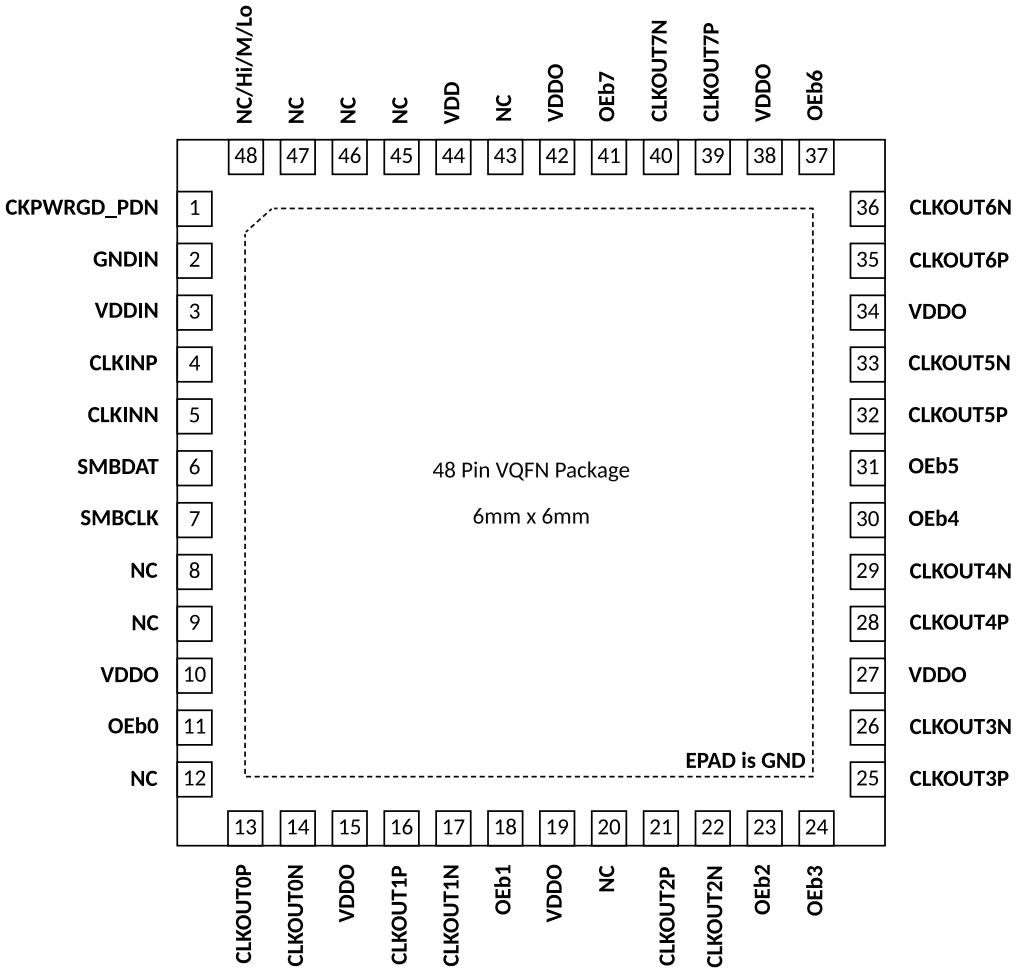


Figure 2. Pin Configuration

Table 9. Pin Description

Pin Name	Pin No.	I/O Type	Description
CKPWRGD_PDN	1	I	3.3 V Input notifies device to sample latched inputs and start up on first high assertion or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
GNDIN	2	Ground	Differential Input clock (receiver) GND
VDDIN	3	PWR	3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
CLKINP	4	I	0.75 V Differential True input
CLKINN	5	I	0.75 V Differential Complementary Input
SADR0	-	I, PD*	SMBUS address strap pin. There is a 3 level input decoding on this pad
SMBDAT	6	I/O	Data pin of SMBUS circuitry, 3.3 V tolerant
SMBCLK	7	I	Clock pin of SMBUS circuitry, 3.3 V tolerant
NC/Hi/M/Lo	48	N/A	This pin does not have any specific user function. NC or any static level will be acceptable.
NC	8, 9, 12, 20,43,45, 46,47	N/A	No Connection. Recommended to be grounded.
VDDO	10, 15, 19, 27, 34, 38, 42	PWR	Power Supply for the Output Drivers, nominal 3.3 V
OEb0	11	I	Active low input for enabling Clock pair 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT0P	13	O	0.75 V differential true clock output

Pin Name	Pin No.	I/O Type	Description
CLKOUT0N	14	O	0.75 V differential Complementary clock output
CLKOUT1P	16	O	0.75 V differential true clock output
CLKOUT1N	17	O	0.75 V differential Complementary clock output
OEb1	18	I	Active low input for enabling Clock pair 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT2P	21	O	0.75 V differential true clock output
CLKOUT2N	22	O	0.75 V differential Complementary clock output
OEb2	23	I	Active low input for enabling Clock pair 2. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
OEb3	24	I	Active low input for enabling Clock pair 3. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT3P	25	O	0.75 V differential true clock output
CLKOUT3N	26	O	0.75 V differential Complementary clock output
CLKOUT4P	28	O	0.75 V differential true clock output
CLKOUT4N	29	O	0.75 V differential Complementary clock output
OEb4	30	I	Active low input for enabling Clock pair 4. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
OEb5	31	I	Active low input for enabling Clock pair 5. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT5P	32	O	0.75 V differential true clock output
CLKOUT5N	33	O	0.75 V differential Complementary clock output
CLKOUT6P	35	O	0.75 V differential true clock output
CLKOUT6N	36	O	0.75 V differential Complementary clock output
OEb6	37	I	Active low input for enabling Clock pair 6. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT7P	39	O	0.75 V differential true clock output
CLKOUT7N	40	O	0.75 V differential Complementary clock output
OEb7	41	I	Active low input for enabling Clock pair 7. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
VDD	44	PWR	3.3 V power for the Core Supply.

Note:

1. PU/PD is weak Pull Up/Pull down with 120 kΩ resistor

Functional Description

Typical Application

Figure 3 shows a SiT92318 typical application. In this application, a clock generator provides a 100-MHz reference to the SiT92318 which then distributes that clock to PCIe endpoints. The clock generator may either be a discrete clock generator, or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

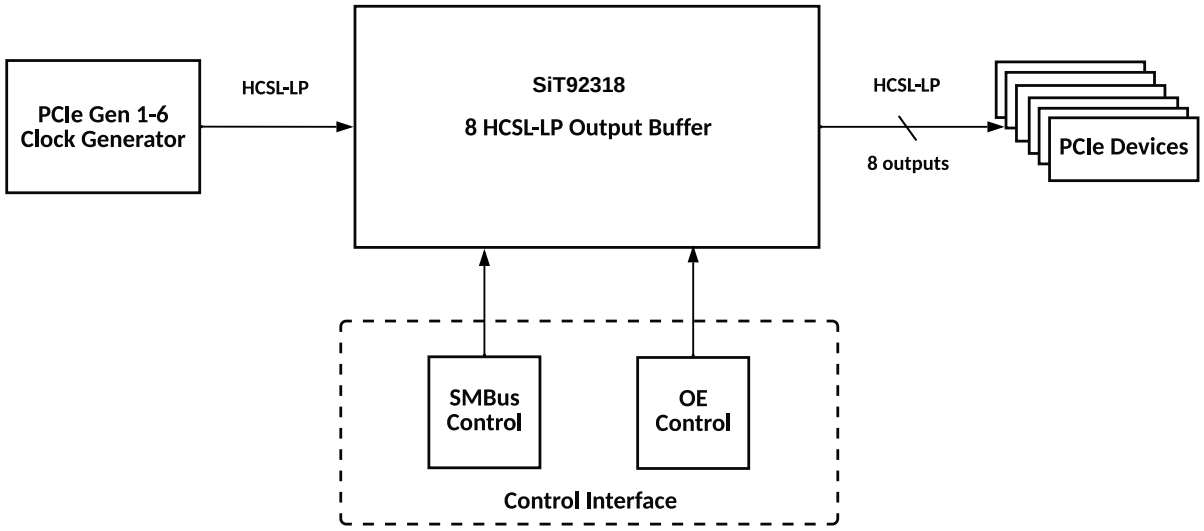


Figure 3. Typical Application Diagram

Parameter Measurement Information

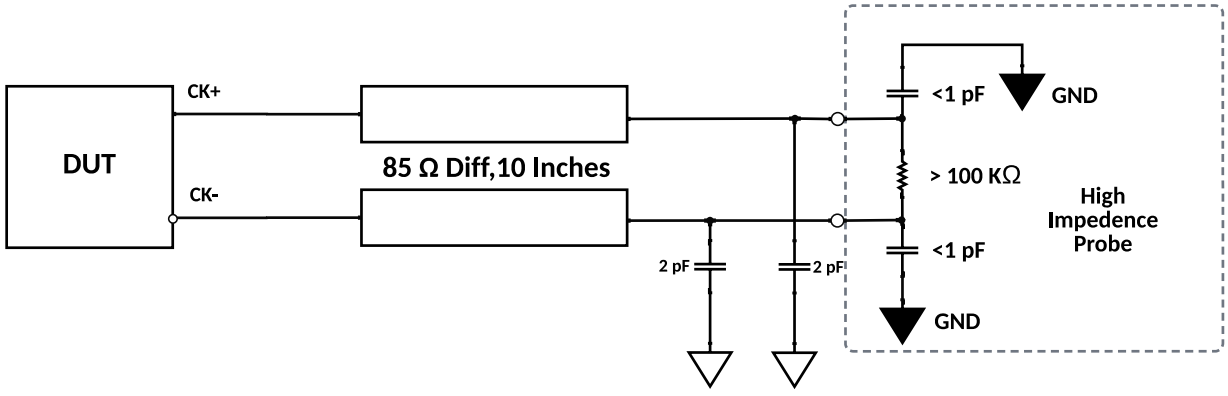


Figure 4. AC Test Mode

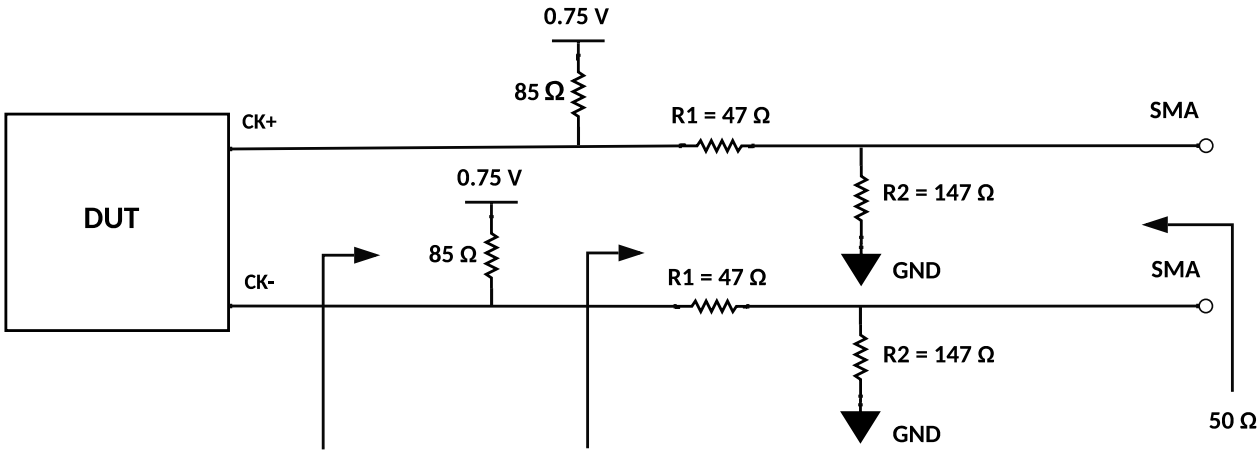


Figure 5. DC Simulation Mode

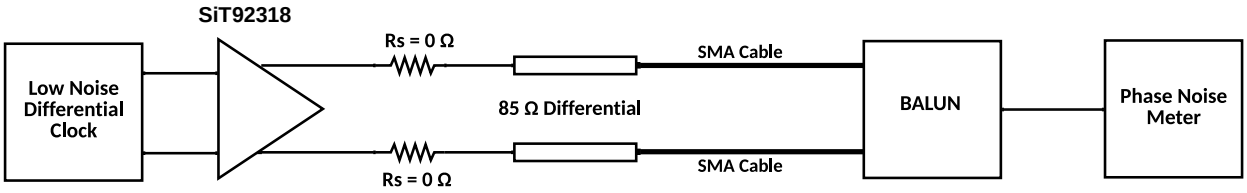


Figure 6. Phase Noise Measurement Setup

Table 10. Input vs Output States

Control Inputs	CLKIN	OEb[7:0] HARDWARE PINS AND SMBus CONTROL REGISTER BIT			CLKOUT[7:0]_P / CLKOUT[7:0]_N
CKPWRGD_PDN		OE[7:0]b Pin	OUT_EN_CLK[7:0]	STOP_STATE_CONFIG_REG	
1	X	X	0	0	LOW/LOW
				1	HiZ/HiZ
				2	High/Low
				3	Low/High
		1	X	0	LOW/LOW
				1	HiZ/HiZ
				2	High/Low
				3	Low/High
	Running	0	1	X	Output Follow input
0	X	X	X	0	LOW/LOW
				1	HiZ/HiZ
				2	High/Low
				3	Low/High

Power Good Assertion and De-assertion

Power Good (CKPWRGD_PDN) is asserted high and de-asserted low. De-assertion of CKPWRGD_PDN (pulling the signal low) is equivalent to indicating a powerdown condition. CKPWRGD_PDN (assertion) is used by the DB800Z to sample initial configurations such as SA selections.

After CKPWRGD_PDN has been asserted high for the first time, the pin becomes a PWRDNb (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDNb is a completely asynchronous active low input.

When entering power savings mode, PWRDNb should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDNb is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

NOTE: The assertion and de-assertion of PWRDNb is asynchronous.

Warning: Disabling of the CLKIN input clock prior to the assertion of PWRDNb is an undefined
mode and is not recommended. Operation in this mode may result in glitches.

Power Good De-Assertion

When PWRDNb is sampled low by two consecutive rising edges of CLKINN, all differential outputs must be held Tri-stated on the next CLKINN high to low transition.

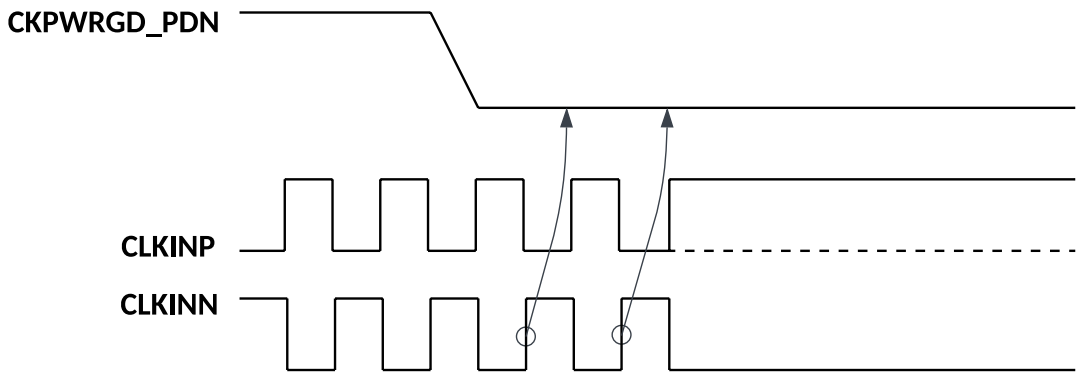


Figure 7. Power Good Assertion

Power Good Assertion

CKPWRGD_PDN must not be asserted to the clock buffer before VDD reaches VDD_{MIN}. Prior to VDD_{MIN} it is recommended to hold PWRGD low (less than 0.5 V).

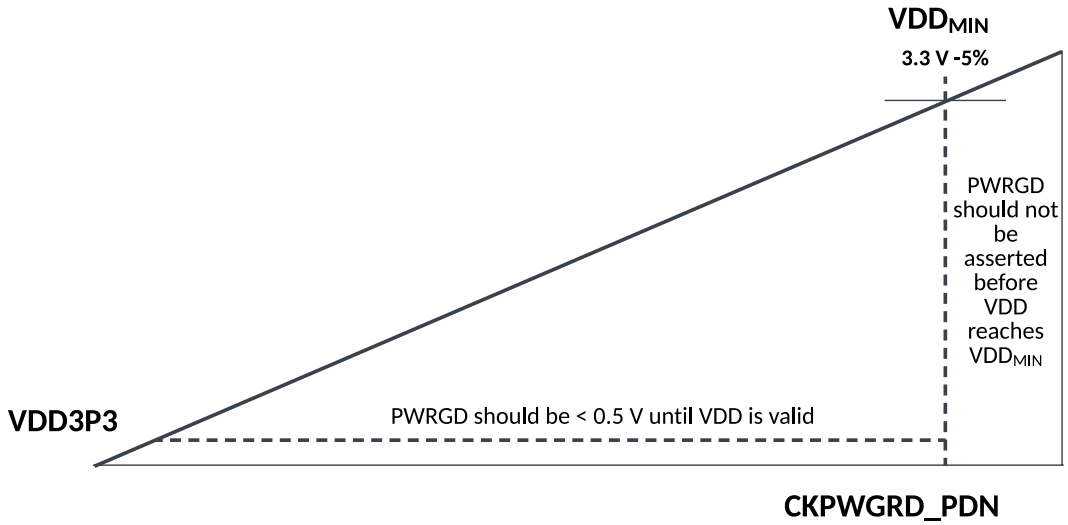


Figure 8. Power Good vs VDD3P3 relationship

The power-up latency in T_{STABLE} is to be less than 1.8 ms. This is the time from the valid CLKINx input and the assertion of the PWRGD signal until the output of the stable clocks from the buffer chip.

All differential outputs stopped in a Tri-state condition resulting from power down must be driven high in less than 300 µs of the PWRGD assertion to a voltage greater than 200 mV.

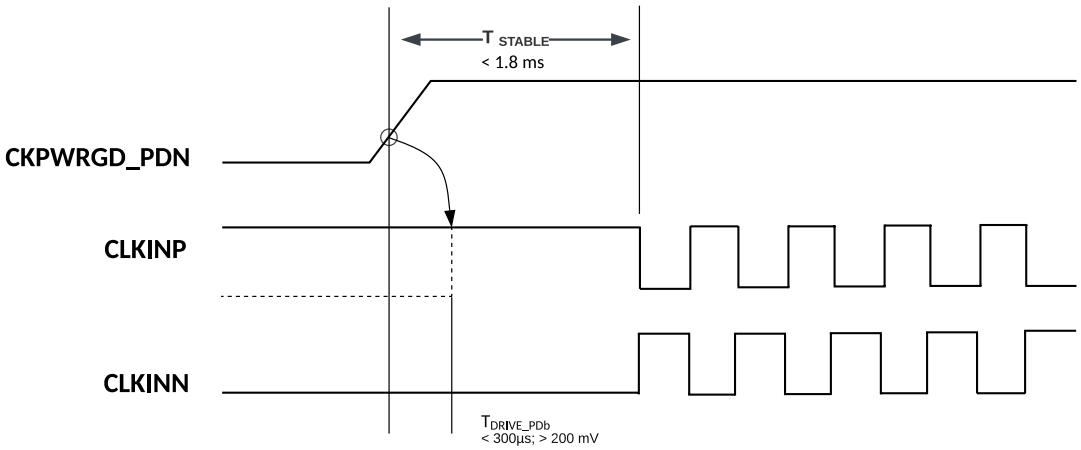


Figure 9. Power Good Assertion

SMBus Parameters

Table 11. SMBus Timing

VDDIN, VDDO = 3.3 V ±5%, -40°C ≤ T_A ≤ 105°C. Typical values are at VDDO = VDDIN= 3.3 V, 25°C (unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SMBus operating Frequency		f_{SMB}	10		400	kHz
Bus Free time between Stop and Start		t_{BUF}				µs
Start Condition hold time	SMBCLK low after SMBDAT low	t_{HD_STA}				
Start Condition setup time	SMBCLK high before SMBDAT low	t_{SU_STA}				
Stop Condition setup time		t_{SU_STO}				
SMBDAT hold time		t_{HD_DAT}				ns
SMBDAT setup time		t_{SU_DAT}				
SMBCLK low timeout detect	Device input clock frequency	$t_{TIMEOUT}$				Cycles
SMBCLK low period		t_{LOW}				µs
SMBCLK high period		t_{HIGH}				
SMBCLK/SMBDAT fall time	Min V_{IH} +0.15 V to Max V_{IL} - 0.15 V	t_F				ns
SMBCLK/SMBDAT rise time	Max V_{IL} -0.15 V to Min V_{IH} +0.15 V	t_R				

Register Address

Table 12. Register Map Address

Register Address	Bit Range	Register name	Default	Type	Bit Name	Description and Function
0x00	7:0	RCR1	0	RO	RESERVED	
0x01	7	OE_CTRL 1	1	RW	DIF5_ENABLE	1: Output Enable 0: STOP_STATE Mode
	6		1		DIF4_ENABLE	
	5		1		DIF3_ENABLE	
	4		1		DIF2_ENABLE	
	3		0		RESERVED	
	2		1		DIF1_ENABLE	
	1		1		DIF0_ENABLE	
	0		0		RESERVED	
0x02	7:3	OE_CTRL 2	0	RW	RESERVED	1: Output Enable 0: STOP_STATE Mode
	2		1		DIF7_ENABLE	
	1		0		RESERVED	
	0		1		DIF6_ENABLE	
0x03	7:0	RCR2	0	RO	RESERVED	
0x04	7:0	RCR3	0	RO	RESERVED	
0x05	7:4	VEN_REV_ID	0	RO	REVISION_ID	0000: revA
	3:0		0		VENDOR_ID	0000: SiTime product
0x06	7:0	DEV_ID	0	RO	DEVICE_ID	Device ID bits[7:0] map to register bits[7:0] directly. Product Code
0x07	7:5	BYTES_READ_COUNT	0	RO	RESERVED	
	4:0		8	RW	BYTES_READ_COUNT_VALUE	Writing to this register configures how many bytes will be read back on a block
0x10	7	OE_PIN_READ_BACK	0	RO	RB_OE7	Output Enableb Pin read Back
	6		0		RB_OE6	
	5		0		RB_OE5	
	4		0		RE_OE4	
	3		0		RB_OE3	
	2		0		RB_OE2	
	1		0		RB_OE1	
	0		0		RB_OE0	
0x14	7:2	STOP_STATE_CONFIG_REG	0	RO	RESERVED	
	1:0		0	RW	STOP_STATE	00 = Low/Low 01 = Hiz/Hiz 10 = High/Low 11 Low/High

Package Dimensions and Patterns

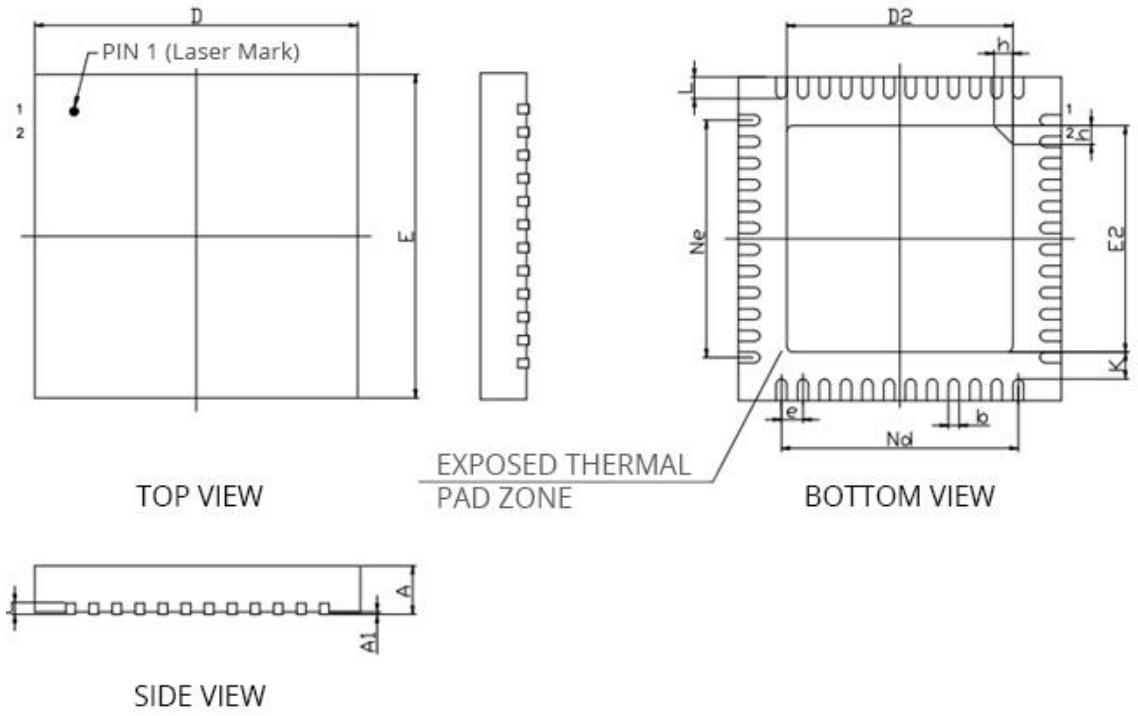


Figure 10. Package Diagram SiT92318 48 pin VQFN

Symbol	Millimeter		
	MIN	NOM	MAX
A	0.80	0.85	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40 BSC		
Ne	4.40 BSC		
Nd	4.40 BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
K	0.20	0.50	0.55
h	0.30	0.35	0.40

Table 13. Revision History

Revisions	Release Date	Change Summary
0.5	11-Dec-2023	Initial Release
0.51	9-Jan-2025	Updated with “P” reel code Updated datasheet format

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