SiT92206

6 Output, Differential, Ultra Low Jitter Buffer

PRELIMINARY

Description

The SiT92206 is a 2.1 GHz, 6 output low-jitter clock fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution and level translation.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock can be distributed to two output drive banks A, B and one LVCMOS output.

The crystal input can support crystals from 8 MHz to 50 MHz. It can also support single ended clock.

The output drivers of each bank can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized to selected clock and can be enabled or disabled in a glitch free manner.

The SiT92206 operates from a 3.3 V/2.5 V core supply and 3 independent 3.3 V/2.5 V output supplies. LVCMOS output driver can be operated at 1.8 V.

Features

- Additive jitter performance of 55 fs RMS
- 3:1 input clock selection
- Two universal clock inputs can operate up to 2.1 GHz and accept LVPECL, LVDS, LVCMOS, CML(ac-coupled only), HCSL, SSTL or single ended clocks
- One crystal input which can support crystals in the frequency range of 8 MHz to 50 MHz or it can accept single ended input clock
- Two output driver banks A and B which can be programmed independently to LVPECL, LVDS, HCSL or HIZ mode
- Typical output skew between clock outputs is 30 ps
- Level translation with core supply voltage of 3.3 V/2.5 V and 3.3 V/2.5 V output supply for differential output drivers (1.8 V support for HCSL driver)
- 3.3 V/2.5 V/1.8 V operation for the single LVCMOS output driver
- The SiT92206 buffer is pin controlled
- High PSRR -70/-73 dBc for LVPECL/LVDS modes
- Supports PCIe Gen1 to Gen5
- SiT92206 is available in a 36-pin, 6 mm x 6 mm QFN package

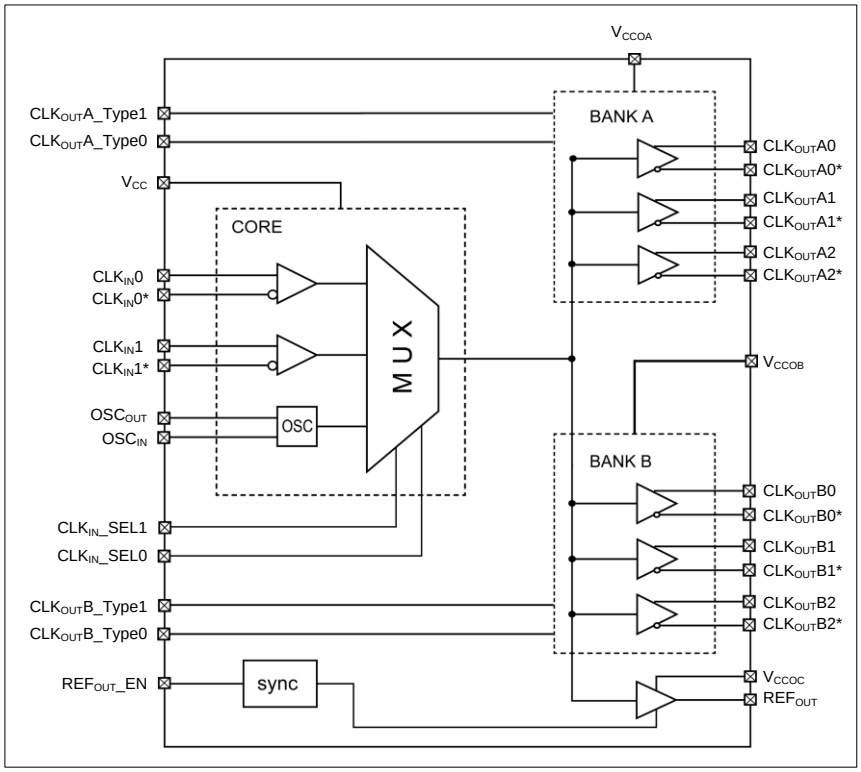

Figure 1. SiT92206 Block Diagram

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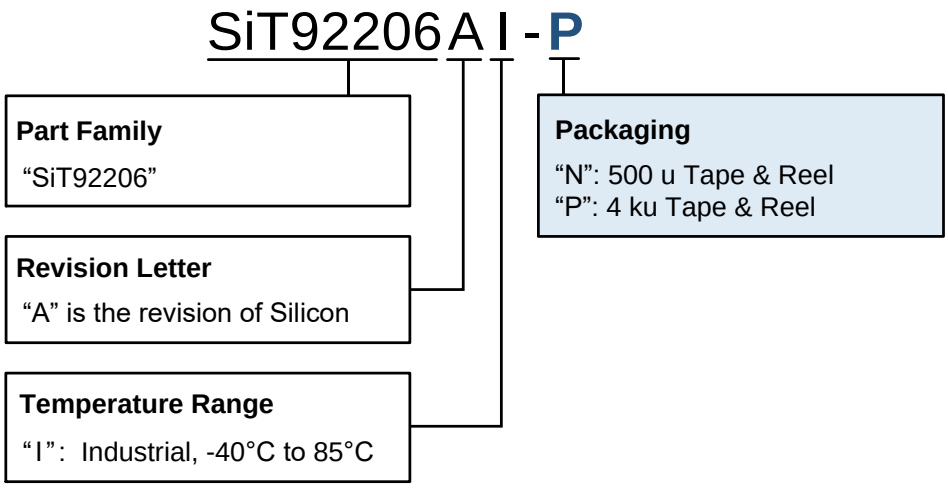
Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings[1,2]

Parameters	Symbol	Min	Typ	Max	Units
Core supply voltage, Analog Input	V_{CC}	-0.3		3.6	V
Output bank supply voltage	V_{CCO}	-0.3		3.6	V
Input voltage, All Inputs, except OSC_{IN}	V_{IN}	-0.3		3.6	V
OSC_{IN}	V_{IN}	-0.5		1.8	V
Storage temperature	T_S	-55		150	°C
Moisture Saturation Level	MSL		3		

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Units
Core supply voltage	V_{CC}	3.135	3.3	3.45	V
	V_{CC}	2.375	2.5	2.625	V
Output supply voltage	$V_{CCOA/B}$	3.135	3.3	3.45	V
	$V_{CCOA/B}$	2.375	2.5	2.625	V
	$V_{CCOA/B}$[1]	1.71	1.8	1.89	V
Output supply voltage for LVCMOS driver	V_{CCOC}	3.135	3.3	3.45	V
Output supply voltage	V_{CCOC}	2.375	2.5	2.625	V
Output supply voltage	V_{CCOC}	1.71	1.8	1.89	V
Ambient Temperature	T_A	-40		85	°C
Junction Temperature	T_J			125	°C

Note:

1. Only for HCSL.

Table 3. Electrical Characteristics

Unless otherwise specified: Vcc = 3.3 V ±5%, 2.5 V ±5%,Vcco = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ TA ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, TA = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Current Consumption						
Core supply current when input buffer is selected	CLK_{IN}0/1 selected, V_{CC} = 3.3 V/2.5 V ± 5%, V_{CC} = V_{CCO}	I_{CC_CORE}		16.5	19.8	mA
Core supply current when Crystal is selected	XO selected, V_{CC} = 3.3 V/2.5 V ± 5%, V_{CC} = V_{CCO}	I_{CORE_XO}(4)			14	mA
Increment in core supply when all ODR banks are enabled		$I_{CC\_ODR\_EN}$			2	mA
Frequency dependent current both bank on core supply. This current scales with frequency	For F_{IN} = 2100 MHz	I_{CC_DYN}(1)(4)		25	33	mA
Additive output supply current per LVPECL bank enabled		I_{CCO_PECL}		109	130.8	mA
Additive output supply current per LVDS bank enabled		I_{CCO_LVDS}		40	49	mA
Additive output supply current per HCSL bank enabled		I_{CCO_HCSL}		76	91.2	mA

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive output supply current, LVCMOS Output Enabled	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 3.3 V	I_{CCO_CMOS}		6	7.2	mA
	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 2.5 V			4.5	5.5	mA
Power Supply Rejection Ratio						
Ripple induced phase spur level, supply ripple of 100 mV pp	F_{IN} = 156.25 MHz, Foffset = 100 KHz $V_{CCOA/B}$ = 2.5 V	$PSRR_{PECL}$		-67		dBc
Ripple induced phase spur level, supply ripple of 100 mV pp	F_{IN} = 156.25 MHz, Foffset = 100 KHz $V_{CCOA/B}$=2.5 V	$PSRR_{LVDS}$		-70		dBc
Ripple induced phase spur level, supply ripple of 100 mV pp	F_{IN} = 156.25 MHz, Foffset = 100 KHz $V_{CCOA/B}$ = 2.5 V	$PSRR_{HCSL}$		-67.7		dBc
Input High Current	V_{CC} = 3.3V, V_{IH} = V_{CC}	I_{IH}		30	50	µA
Input Control Pin Characteristic						
Input Low Current		I_{IL}	-20	0.1		µA
Input high voltage – Logic inputs		V_{IH}	0.7*V_{CC}		V_{CC}	V
Input low voltage – Logic inputs		V_{IL}	GND		0.3*V_{CC}	V
Internal Pull-down resistance		$R_{pulldown}$		200		K Ω

Notes:

1. Total current from core supply at frequency F_{IN} = $I_{CORE, STATIC}$ + N*(0.5*F_{IN}/2100M)* $I_{CORE, DYN}$. Detailed methodology of calculating the power dissipated in each ODR mode is given in the section “Current consumption and Power Dissipation Calculations.” N is the number of output banks enabled.
2. Refer to Application Information section for more information on current consumption and power dissipation calculations.
3. Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 * 10(PSRR / 20)) / (π * f_{CLK})] * $1E^{12}$
4. Specification is ensured by characterization and is not tested in production.

Table 4. Input Clock Characteristics

Unless otherwise specified: Vcc = 3.3 V ±5%, 2.5 V ±5%, Vcco = 3.3 V ±5%, 2.5 V ±5%, -40 °C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Characteristics of Universal Input Clock Pins						
Input frequency range[4]		F_{CLKin} [1]	DC		2100	MHz
Differential input high voltage	CLK_{IN} driven differentially	V_{IHD}			V_{CC}	V
Differential input low voltage		V_{ILD}	GND			V
Peak differential input voltage swing(2)		V_{ID}	0.15		1.3	V
Differential input common mode voltage	Input differential swing of 150 mV	V_{CMD}	0.25		V_{CC}-1.2	V
	Input differential swing of 350 mV		0.25		V_{CC}-1.1	V
	Input differential swing of 800 mV		0.25		V_{CC}-0.9	V
Single ended input high voltage	Inverting differential input held at V_{CC}/2, V_{CC} = 3.3 V	V_{IH}	2		V_{CC}	V
	Inverting differential input held at V_{CC}/2, V_{CC} = 2.5 V		1.6		V_{CC}	
Single ended input low voltage	Inverting differential input held at V_{CC}/2, V_{CC} = 3.3 V	V_{IL}	GND		1.3	V
	Inverting differential input held at V_{CC}/2, V_{CC} = 2.5 V		GND		0.9	

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Single ended input voltage swing [3]		V_{I_SE}	0.3		2	VPP
Single ended input common mode voltage		V_{CM}	0.25		V_{CC}-1.2	V
Mux Isolation between the two input clock paths	F_{IN} = 100 MHz, Foffset > 50 KHz	ISO_{MUX} [1]		-84		dBc
	F_{IN} = 200 MHz, Foffset > 50 KHz			-82		dBc
	F_{IN} = 500 MHz, Foffset > 50 KHz			-71		dBc
	F_{IN} = 1000 MHz, Foffset > 50 KHz			-65		dBc
Crystal Characteristics						
Equivalent series resistance		ESR		35	60	Ω
Load capacitance		CL	6	8	10	pF
Shunt Capacitance		Co		2	3	pF
Power dissipated in the crystal		Drive level		100	200	uW
Mode of oscillation			Fundamental			
Crystal frequency range		F_{OSC} [1]	8		50	MHz
External clock frequency range	XO over drive or Bypass mode	F_{CLK}			250	MHz
Maximum swing level on OSC_{IN}/OSC_{OUT} pins	XO over drive or Bypass mode	Vmax			1.8	Vpp_se
Vih_se	Bypass DC coupled mode. SEL[1] = 1 & SEL[0]=1	Vih	0.98			V
Vil_se		Vil			0.36	V
Crystal Phase jitter [5]	RMS, integration BW 12 KHz to 5 MHz, $F_{crystal}$ = 25 MHz. Crystal input select Measured at V_{CC} = V_{CCO} = 2.5 V	t_{jit} [1]		155		fs

Notes:

1. Specification is ensured by characterization and is not tested in production.
2. Refer to Parameter Measurement Information section for definition of VID and VOD voltages.
3. For clock input frequency ≥ 100 MHz, CLKinX can be driven with single-ended (LVCMOS) input swing up to 3.3 Vpp. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 Vpp max to prevent input saturation (refer to Driving the Clock Inputs for interfacing 2.5 V/3.3 V LVCMOS clock input < 100 MHz to CLK_{IN}X).
4. If the input clock is initially absent when the chip is just powered up, it will take atleast 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock
5. Crystal Phase Jitter is measure on following part number, 7M-25.000MAKV-T.

Table 5. Output Clock Characteristics – LVPECL

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C. Termination is 50 Ω to V_{CCO} -2 V.

Parameters	Condition	Symbol	Min	Typ	Max	Unit
Maximum output frequency, full VOD swing ≥ 600 mV[1]	50 Ω termination biased with V_{CCO} -2V	F_{CLKOUT_F}[1]	1000	1200	-	MHz
Maximum output frequency, full VOD swing ≥ 400 mV[1]			1500	2100		MHz
Additive RMS jitter[1]	Integration bandwidth from 10 KHz to 20 MHz, F_{IN} = 156.25 MHz, SR > 3 V/ns 50 Ω termination biased with V_{CCO} -2V	$Jitter_{ADD}$[1]		55		fs(rms)

Parameters	Condition	Symbol	Min	Typ	Max	Unit
Noise floor for Foffset > 10 MHz	50 Ω termination biased with V_{CCO}-2V, F_{IN} = 156.25 MHz, SR > 3 V/ns	$Noise_{FLOOR}$[1]		-159		dBc
Output Duty Cycle	50 Ω termination biased with V_{CCO} -2V	ODC	45		55	%
Output high voltage	50 Ω termination biased with V_{CCO} -2V	V_{OH}	V_{CCO}– 1.165		V_{CCO} – 0.75	V
Differential output voltage	50 Ω termination biased with V_{CCO} -2V	V_{OD}	475	678	960	mV
Output low voltage	50 Ω termination biased with V_{CCO} -2V	V_{OL}	V_{CCO} – 2.0		V_{CCO} – 1.45	V
Output rise time, 20% to 80%	50 Ω termination biased with V_{CCO} -2V	t_R		210		ps
Output fall time 20% to 80%	50 Ω termination biased with V_{CCO} -2V	t_F		210		ps
Input to output delay	50 Ω termination biased with V_{CCO} -2V	t_{pd}		876	1100	ps

Notes:

1. Specification is guaranteed by characterization and is not tested in production.

Table 6. Output Clock Characteristics - LVDS

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Maximum output frequency, full VOD swing ≥ 250 mV	R_L = 100 Ω, differential	F_{CLKOUT_FS}[1]	1000	1600	-	MHz
Maximum output frequency, full VOD swing ≥ 200 mV	R_L = 100 Ω, differential		1500	2100		MHz
Additive RMS jitter	Integration bandwidth from 10 KHz to 20 MHz, F_{IN} = 156.25 MHz, SR > 3 V/ns R_L = 100 Ω, differential	$Jitter_{ADD}$		60		fs(rms)
Noise floor for Foffset > 10 MHz	F_{IN} = 156.25 MHz, SR > 3 V/ns R_L = 100 Ω, differential	$Noise_{FLOOR}$		-159		dBc
Output Duty Cycle	R_L = 100 Ω, differential	ODC	45		55	%
Change in VPP between complementary output states	R_L = 100 Ω, differential	ΔVPP			50	mV
Output differential peak voltage	R_L = 100 Ω, differential	V_{OD}	247		454	mV
Output Common-Mode Voltage	R_L = 100 Ω, differential	V_{OCM}	1.125	1.2	1.375	V
Output rise time, 20% to 80%	R_L = 100 Ω, differential, C_L < 5 pF	t_R		210		ps
Output fall time 20% to 80%	Uniform transmission line up to 10 inches with characteristic impedance of 50 Ω	t_F		210		ps
Input to output delay		t_{pd}		840	1100	ps
Skew between outputs	V_{CCO} = 3.3 V, 2.5 V	T_{sk}		30		ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 7. Output Clock Characteristics - HCSL

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Maximum output frequency	R_L= 50 Ω to GND	F_{CLKOUT_F} [1]	DC		700	MHz
Additive RMS jitter	Integration bandwidth from 10 KHz to 20 MHz, F_{IN} = 156.25 MHz, SR > 3 V/ns R_L = 50 Ω to GND	$Jitter_{ADD}$ [1]		55		fs(rms)
Noise floor for Foffset > 10 MHz		$Noise_{FLOOR}$ [1]		-159		dBc
Output Duty Cycle		ODC	45		55	%
Output Low Voltage Min	R_L = 50 Ω to GND	V_{MIN}	-300			mV
Differential Output High Voltage		V_{OH}	600	840	1150	mV
Differential Output Low Voltage		V_{OL}	-150	28	150	mV
Absolute Crossing point voltage	R_L = 50 Ω to GND, C_L < 5 pF	V_{CROSS}	250		550	mV
Variation of V_{CROSS} over all rising clock edges		V_{CROSS} DELTA			140	mV
Output rise time, 20% to 80%	F_{IN} = 156.25 MHz, Uniform transmission line up to 10 inches with characterisitic impedance of 50 Ω R_L = 50 Ω to GND, C_L < 5 pF	t_R		210		ps
Output fall time 20% to 80%		t_F		210		ps
Input to output delay		t_{pd}		825	1100	ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 8. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1[1,2,3,4]	$tj_{phPCIeG1-CC}$		2	5	ps (p-p)
	PCIe Gen 2[1,2,3,4]	$tj_{phPCIeG2-CC}$		0.08	0.15	ps(rms)
	PCIe Gen 3[1,2,4,6]	$tj_{phPCIeG3-CC}$		0.03	0.07	ps(rms)
	PCIe Gen4[1,2,4,6]	$tj_{phPCIeG4-CC}$		0.03	0.07	ps(rms)
	PCIe Gen5[1,2,4,6]	$tj_{phPCIeG5-CC}$		0.01	0.02	ps(rms)

Notes:

1. Applies to all the differential outputs, gauranteed by design and characterization.
2. Applies to all the Outputs when driven by a low phase noise source SMA100B.
3. Additive RMS Jitter Measurements were made using DSA90804A for minimum waveform length of ≥ 100k cycles with a minimum sampling rate of ≥ 40GSa/s with the waveform covering 90% of the DSO screen. All the post processing the DSO is disabled to decrease the additonal jitter impact from oscilloscope. Broadband oscilloscope noise is also minimized in the measurement.
4. Additive jitter for RMS values is calculated by solving the equation for b [b=sqrt(c^2-a^2) where ‘a’ the rms input jitter and “c” is the rms total jitter.
5. Input to SiT92206 is fed using low phase noise source SMA100B, SiT92206 is configured as 100 MHz HCSL Output Driver [V_{CCO}x = 3.3 V] and fed to the channels of DSA90804A using the exact measurement set up [Refer Note 6].
6. SiT92206 PCI Express Additive RMS Jitter Measurement Set up configuration.

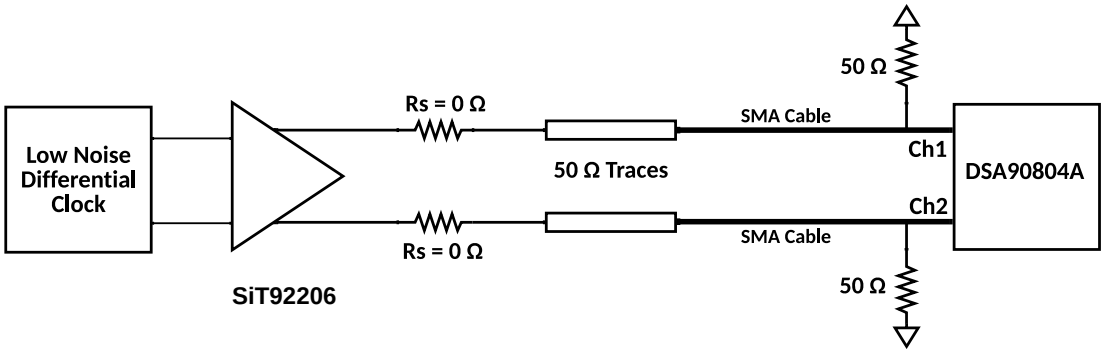


Table 9. Output Clock Characteristics – LVCMOS

Unless otherwise specified: V_{CC} = 3.3 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Frequency		f_{CLKOUT}	0		250	MHz
Additive RMS jitter	V_{CCOC} = 3.3 V ± 5%	$Jitter_{ADD}$[1]		55		fs rms
	V_{CCOC} = 2.5 V ± 5%			63		fs rms
Noise floor for Foffset > 10 MHz V_{CCOC}	V_{CCOC} = 3.3 V ± 5%	$Noise_{FLOOR}$[1]		-159		dBc
	V_{CCOC} = 2.5 V ± 5%			-157		dBc
Output Duty Cycle	For F_{IN} ≤ 200 MHz	ODC	45		55	%
	For 200 MHz < F_{IN} < 250 MHz		40		60	%
Output high voltage	V_{CCOC} = 3.3 V ± 5%, 1 mA pull down current	V_{OH}	V_{CCOC} -0.1 V			V
	V_{CCOC} = 2.5 V ± 5%, 1 mA pull down current		V_{CCOC} -0.1 V			V
Output low voltage	V_{CCOC} = 3.3 V ± 5%, 1 mA pull up current	V_{OL}			0.1	V
	V_{CCOC} = 2.5 V ± 5%, 1 mA pull up current				0.1	V
Output rise time, 20% to 80%	C_{LOAD} = 5 pF, R_{LOAD} = 50 Ω AC coupled	t_R		250	450	ps
Output fall time 20% to 80%		t_F		250	450	ps
Output enable time		t_{EN}[1]			4	cycles
Output disable time		t_{DIS}[1]			4	cycles
Input to clock edge to output clock edge delay	V_{CCO} = 3.3 V, PCB trace of 5 inch, 5 pF capacitor	t_d[1]		1.4	2.5	ns
	V_{CCO} = 2.5 V, PCB trace of 5 inch, 5 pF capacitor			1.5	2.7	ns

Notes:

1. Specification is ensured by characterization and is not tested in production.

Pin Configuration

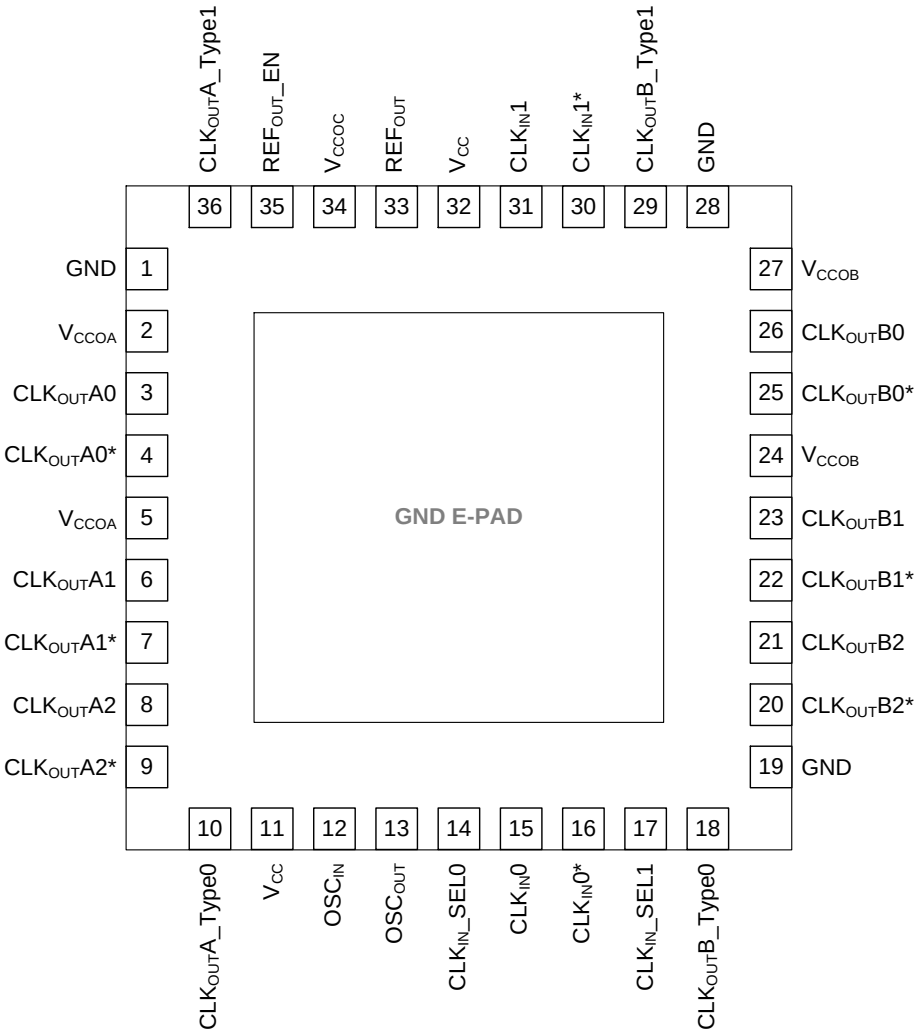


Figure 2. SiT92206 Pin Configuration Top View

Table 10. Pin Description

Pin Number	Pin Name	Functionality SiT92206
Pin group: Bank A clock output pads		
$CLK_{OUT}A0$	3	Differential clock output P of A0. Output type set by $CLK_{OUT}A$_TYPE pins.
$CLK_{OUT}A0*$	4	Differential clock output N of A0. Output type set by $CLK_{OUT}A$_TYPE pins.
$CLK_{OUT}A1$	6	Differential clock output P of A1. Output type set by $CLK_{OUT}A$_TYPE pins.
$CLK_{OUT}A1*$	7	Differential clock output N of A1. Output type set by $CLK_{OUT}A$_TYPE pins.
$CLK_{OUT}A2$	8	Differential clock output P of A2. Output type set by $CLK_{OUT}A$_TYPE pins.
$CLK_{OUT}A2*$	9	Differential clock output N of A2. Output type set by $CLK_{OUT}A$_TYPE pins.
Pin group: Bank B clock output pads		
$CLK_{OUT}B0$	26	Differential clock output P of B0. Output type set by $CLK_{OUT}B$_TYPE pins.
$CLK_{OUT}B0*$	25	Differential clock output N of B0. Output type set by $CLK_{OUT}B$_TYPE pins.
$CLK_{OUT}B1$	23	Differential clock output P of B1. Output type set by $CLK_{OUT}B$_TYPE pins.
$CLK_{OUT}B1*$	22	Differential clock output N of B1. Output type set by $CLK_{OUT}B$_TYPE pins.
$CLK_{OUT}B2$	21	Differential clock output P of B2. Output type set by $CLK_{OUT}B$_TYPE pins.
$CLK_{OUT}B2*$	20	Differential clock output N of B2. Output type set by $CLK_{OUT}B$_TYPE pins.

Pin Number	Pin Name	Functionality SiT92206
Pin group: Bank C clock output pad		
REF_{OUT}	33	LVCMOS clock out synchronized with differential clocks
Pin group: Clock inputs		
$CLK_{IN}0$	15	Universal clock input 0 (+ve polarity) (differential/single-ended)
$CLK_{IN}0$*	16	Universal clock input 0 (-ve polarity) (differential/single-ended)
$CLK_{IN}1$	31	Universal clock input 1 (+ve polarity) (differential/single-ended)
$CLK_{IN}1$*	30	Universal clock input 1 (-ve polarity) (differential/single-ended)
OSC_{IN}	12	Input for crystal. It can be over driven by an AC coupled single ended clock in crystal over drive mode. In the external bypass mode, the max voltage at the pin needs to be 1.5 V. If the dirver is swinging to say 3.3 V rail, then a resistor divider is needed on PCB to restrict the swing at OSC_{IN} to 1.5V Cload supported 6 pF to 10 pF, freq 8 MHz to 50 MHz
OSC_{OUT}	13	Output for crystal. Leave OSC_{OUT} floating if OSC_{IN} is driven by a single-ended clock.
Pin group: Power pins		
V_{CC}	11	Line supply - 3.3 V/2.5 V
V_{CC}	32	Line supply - 3.3 V/2.5 V
V_{CCOA}	2	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3 V or 2.5 V
V_{CCOA}	5	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3 V or 2.5 V
V_{CCOB}	27	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3 V or 2.5 V
V_{CCOB}	24	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3 V or 2.5 V
V_{CCOC}	34	Power supply for Bank C Output buffer. V_{CCOC} can operate from 3.3 V or 2.5 V or 1.8 V
GND-EPAD	0	Ground
GND	19	Ground pin
GND	28	Ground pin
GND	1	Ground pin
Pin group: Control pins		
CLK_{OUT}A_Type0	10	Bank A output buffer type selection pins
CLK_{OUT}A_Type1	36	Bank A output buffer type selection pins
CLK_{OUT}B_Type0	18	Bank B output buffer type selection pins
CLK_{OUT}B_Type1	29	Bank B output buffer type selection pins
REF_{OUT}_EN	35	REF_{OUT} enable input. Enable signal is internally synchronized to selected clock input.
CLK_{IN}_SEL0	14	Clock input selection pins
CLK_{IN}_SEL1	17	Clock input selection pins

Functional Description

The SiT92206 is a 6-output differential clock fan out buffer with low additive jitter that can operate up to 2.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 3 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 36-pin WQFN package.

V_{CC} and V_{CCO} Power Supplies

The SiT92206 has separate 3.3/2.5 core (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}). HCSL can support 1.8V power supplies (V_{CCOA}, V_{CCOB}). VCCOC supply can operate on 3.3 V/2.5 V/1.8 V rail. Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective V_{CCO} supply, while the output levels for LVDS and HCSL are relatively constant over the specified V_{CCO} range.

Clock Inputs

The input clock can be selected from $CLK_{IN}0/CLK_{IN}0^*$, $CLK_{IN}1/CLK_{IN}1^*$, or OSC_{IN}. Clock input selection is controlled using the CLK_{IN}_SEL[1:0] inputs as shown in Table 11. When $CLK_{IN}0$ or $CLK_{IN}1$ are selected, the oscillator is power down. The user can float OSC_{IN} and OSC_{OUT} pins, since these pins are internally pulled down. OSC_{IN} is pulled down with a 56 KΩ resistance.

Table 11 Input Clock Selection

CLK_{IN}_SEL[1]	CLK_{IN}_SEL[0]	Selected Clock
0	0	$CLK_{IN}0$, $CLK_{IN}0^*$
0	1	$CLK_{IN}1$, $CLK_{IN}1^*$
1	0	Crystal Or Crystal Bypass AC Coupled mode
1	1	Crystal Bypass DC Coupled mode

Clock States (Input vs Output States)

Table 12. Input versus Output Stages

State of Selected Clock input	Output State
Inputs are floating	Logic low
Inputs are logic low	Logic low
Inputs are logic high	Logic high

Output Driver Type

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the CLK_{OUT}A_TYPE[1:0] and CLK_{OUT}B_TYPE[1:0] inputs, respectively, as shown Table 13. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power.

Table 13. OE Functionality

CLK_{OUT}X_TYPE1	CLK_{OUT}X_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

Reference Output

The reference output (REF_{OUT}) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the V_{CCOC} voltage. REF_{OUT} can be enabled or disabled using the enable input pin, REF_{OUT}_EN, as shown in Table 14. The reference output clock is internally synchronized to the selected clock. This avoids any glitches or runt pulses while enabling or disabling the reference clock. Pulling REF_{OUT}_EN to LOW, forces the outputs to the high-impedance state with in 4 falling edges of the input signal. The outputs remain in the high-impedance state as long as REF_{OUT}_EN is LOW. When REF_{OUT}_EN goes from HIGH to LOW, the output clock is disabled within 4 falling edges of the input clock signal. The output is disabled at the falling edge of the input clock. This allows to disable the output clock in a glitch free manner.
When REF_{OUT}_EN goes from low to high, the output clock is enabled within a time delay td, where td is given by the following equation.

$$t_{d,refout\_en} = 0.5n + 3 * Tin.$$

Where, Tin is the time period of the input clock.

When REF_{OUT}_EN is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REF_{OUT}_EN is configured with a 1K Ω load to ground, then the output will be pulled to low when disabled.

Table 14. Reference Output Enable

Ref_{OUT}_EN	Output State
0	Disabled (HiZ)
1	Enabled

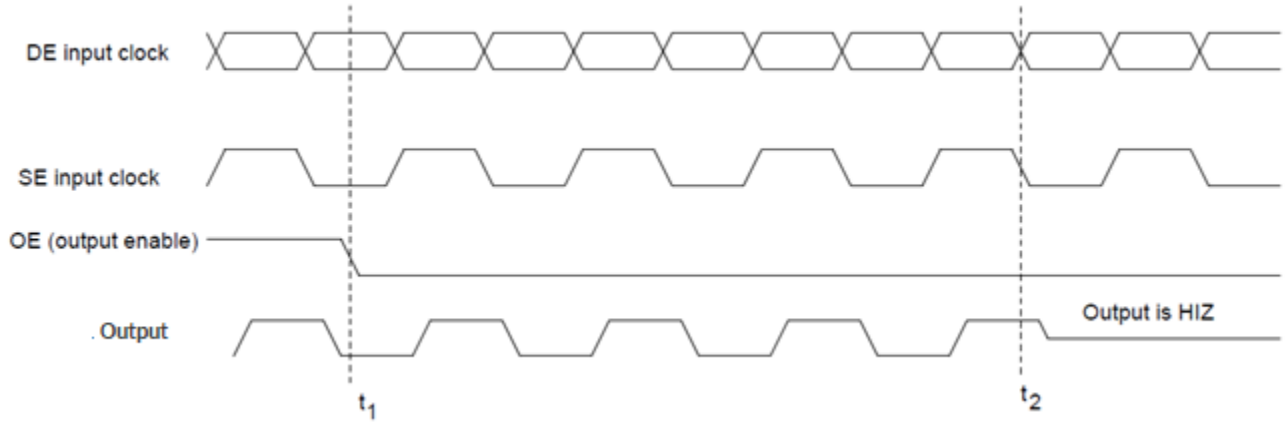


Figure 3. REF$_{OUT}$_EN: Output disable

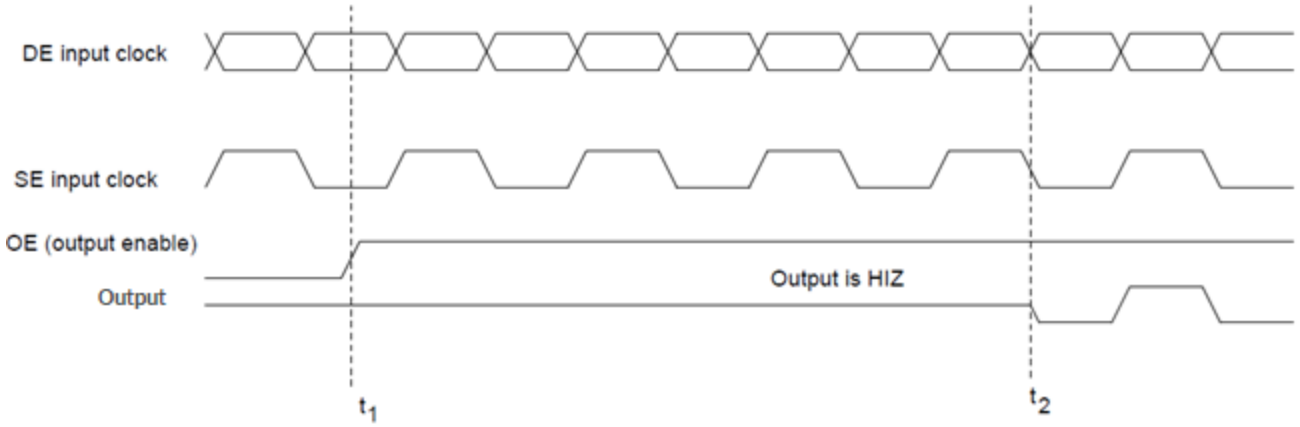


Figure 4. REF$_{OUT}$_EN: Output enable

Application Information

Current consumption and Power Dissipation Calculations

The current consumption specified in the Electrical Characteristics can be used to calculate the total power dissipation and the IC power dissipation for any output driver configuration. The total current drawn from the V_{CC} is given by the equation below.

$$I_{CC} = I_{CORE,STATIC} + n * \left(\frac{f_{in}}{100}\right) * I_{CORE,DYN}$$

- I_{CC}, is the total core current drawn from V_{CC}.
- $I_{CORE,STATIC}$, is the current drawn by SiT92206, when clocks are not toggling and both the output driver banks are in HIZ state.
- $I_{CORE,DYN}$, is the switching current taken from V_{CC} when the selected input clock is toggling at a frequency of f_{in}.
- n, is the number of output banks that are active.

Current consumed by the output supplies in each mode are listed below.

- The current in output bank A/B in LVPECL mode is $I_{CCOA} = I_{CCOB} = I_{CC\_LVPECL}$
- The current in output bank A/B in LVDS mode is $I_{CCOA} = I_{CCOB} = I_{CC\_LVDS}$
- The current in output bank A/B in HCSL mode is $I_{CCOA} = I_{CCOB} = I_{CC\_HCSL}$
- The current in output bank C is $I_{CCOC} = I_{CC\_LVCMOS}$

The equation for the total power dissipation is

$$P_{TOTAL} = V_{CC} * I_{VCC} + V_{CCOA} * I_{CCOA} + V_{CCOB} * I_{CCOB} + V_{CCOC} * I_{CCOC}$$

If the output driver configuration is HCSL, LVPECL or LVDS, then the power dissipated in any termination resistors and termination voltages need to be accounted to calculate the power dissipation in the device.
The power dissipated in the termination resistor in LVPECL mode is given below.

$$P_{RT\_PECL} = \frac{\left(V_{OH\_PECL} - V_{TT}\right)^2}{R_T} + \frac{\left(V_{OL\_PECL} - V_{TT}\right)^2}{R_T}$$

The power dissipated in the termination voltage for LVPECL mode is given below

$$P_{VTT\_PECL} = V_{TT} * \left(\frac{\left(V_{OH\_PECL} - V_{TT}\right)}{R_T} + \frac{\left(V_{OL\_PECL} - V_{TT}\right)}{R_T}\right)$$

The power dissipated in the ground referenced termination resistor for HCSL is given below

$$P_{RT\_HCSL} = \frac{V_{OH\_HCSL}^2}{R_T}$$

The power dissipated in the device is given below.

$$P_{DEVICE} = P_{TOTAL} - N_1 * \left(P_{RT_{PECL}} + P_{VTT_{PECL}}\right) - N_2 * P_{RT\_HCSL}$$

Example: Worst case power dissipation

BANK A and BANK B output drivers are configured in HCSL mode. The input frequency is 2100 MHz. V_{CC} = 3.465 V, V_{CCOA} = V_{CCOB} = 3.465 V, REF_{OUT} is disabled.

Table 15. Worst Case Power Dissipation

Parameter	Value	Unit
V_{CC}	3.465	V
V_{CCOA}	3.465	V
V_{CCOB}	3.465	V
V_{CCOC}	3.465	V
I_{CC}	49.2	mA
I_{CCOA}	93	mA
I_{CCOB}	93	mA
P_{TOTAL}	815	mW
V_{OH_HCSL}	0.83	V
V_{OL_HCSL}	0.044	V
$P_{load:}$	119	mW
P_{DEVICE}	696	mW

Driving the Clock Inputs

The SiT92206 has two universal clock inputs ($CLK_{IN}0/CLK_{IN}0^*$ and $CLK_{IN}1/CLK_{IN}1^*$). SiT92206 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The SiT92206 supports a wide common mode voltage range and input signal swing
To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter.
It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say $CLK_{IN}0$, then $CLK_{IN}0^*$ pin need to be connected to a 0.1 uF capacitor on the PCB.

Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 5 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors R_{T1} and R_{T2} set the common mode voltage at the output of the LVCMOS driver to $V_{CC}/2$. This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.
For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center)

of this signal is 1.25 V, the R_{T1} and R_{T2} values should be adjusted to set the V1 at 1.25 V. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

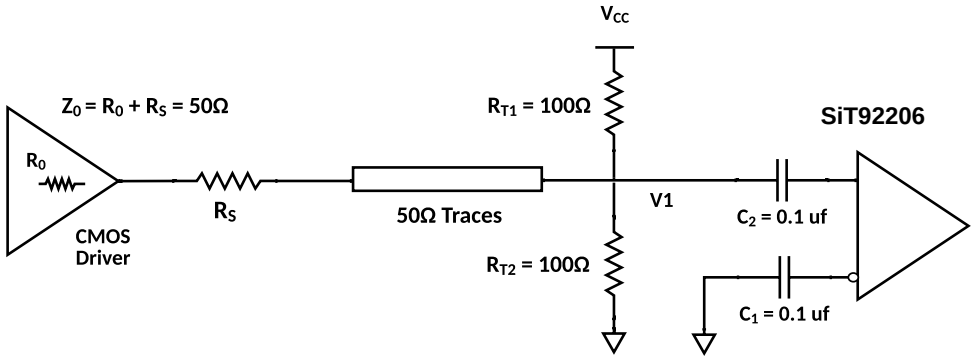


Figure 5. AC coupling LVCMOS clock to SiT92206

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to V_{CC}/2.

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 6. We use single termination resistor of 50 Ω to ground. A 0.1 uF (C_3) ac coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50\ Ohm$$

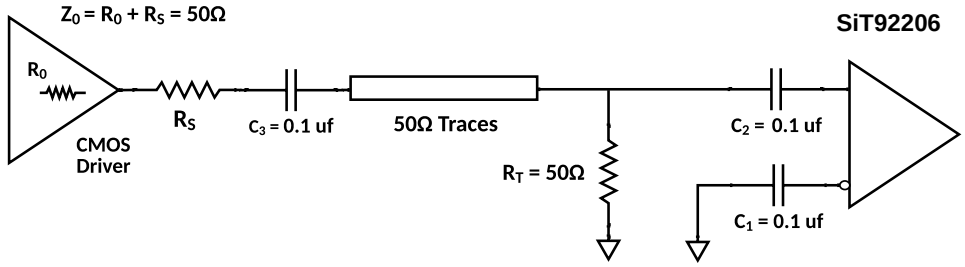


Figure 6. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 7 shows how a differential input can be wired to accept LVCMOS single ended clock signals in DC coupled mode. The reference voltage V1 = V_{CC}/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vcc}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

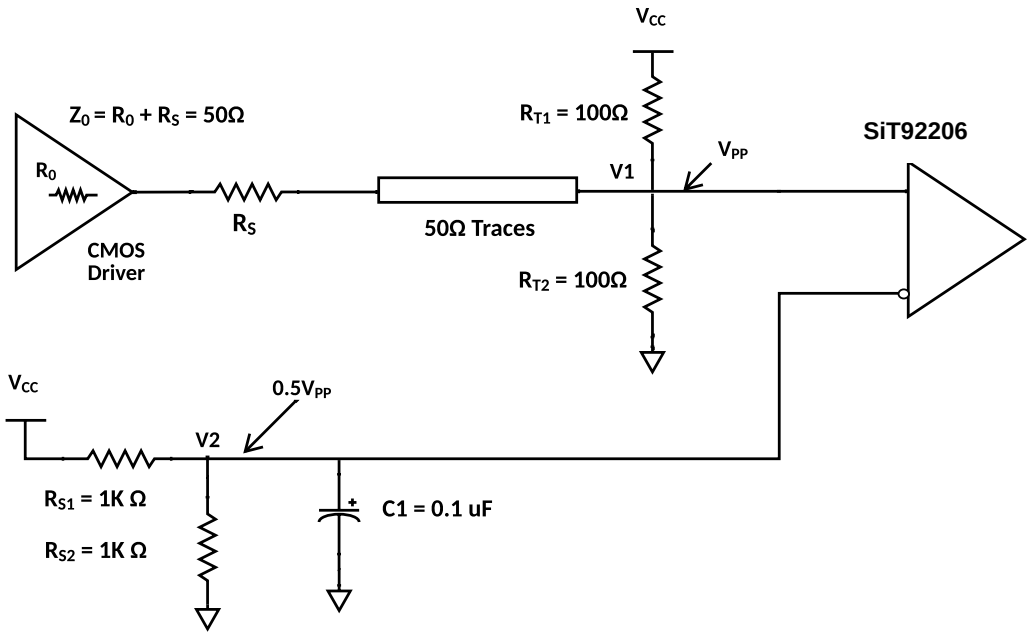


Figure 7. DC coupling of LVCMOS clock to SiT92206 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values given below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 8 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50 Ω load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 8 is given below

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2}$$

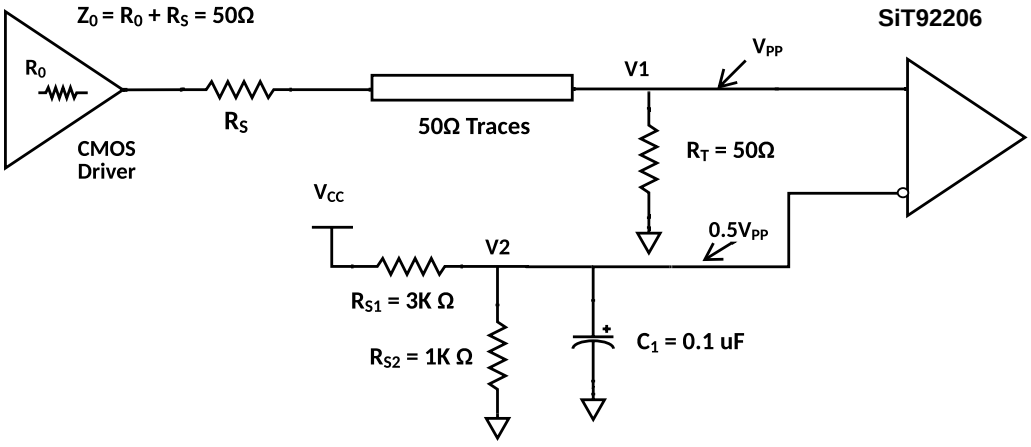


Figure 8. DC coupled LVCMOS input clock configuration – configuration 2

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 9. There is a single termination resistor RT which is connected to ground through a capacitor C_{AC}.

The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega},$$

Where T_D is the transmission line delay

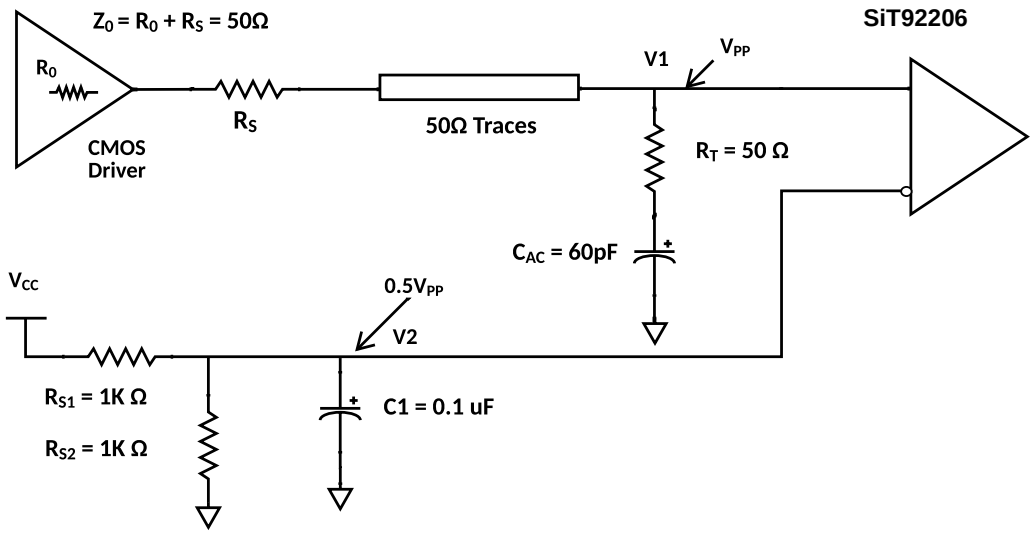


Figure 9. DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to SiT92206 input clock pin as shown in Figure 10.

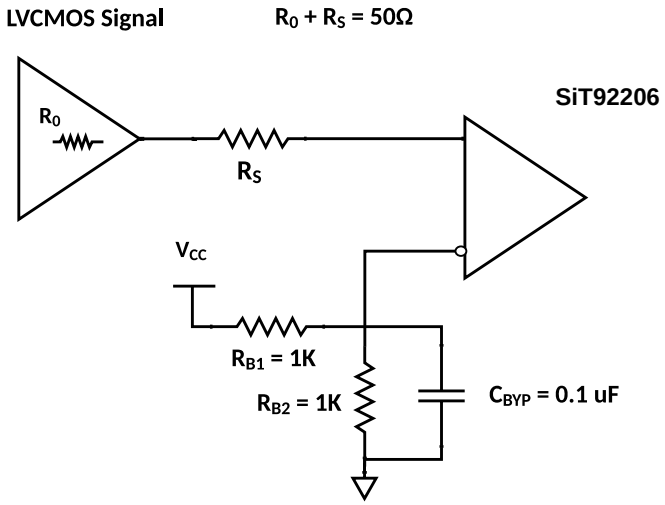


Figure 10. Direct coupling of LVCMOS clock to SiT92206

Driving OSC_{IN} with LVCMOS Driver (AC coupled)

The crystal input OSC_{IN} can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at OSC_{IN} should be limited to 1.8 V. The OSC_{OUT} pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at OSC_{IN} should not exceed 1.8 V and minimum voltage should not go below -0.5 V. The slew rate at OSC_{IN} should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 11 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.8 V. The maximum DC bias voltage of OSC_{IN} is 0.675 V. Therefore the maximum swing at the OSC_{IN} pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.8 = 1.575V$$

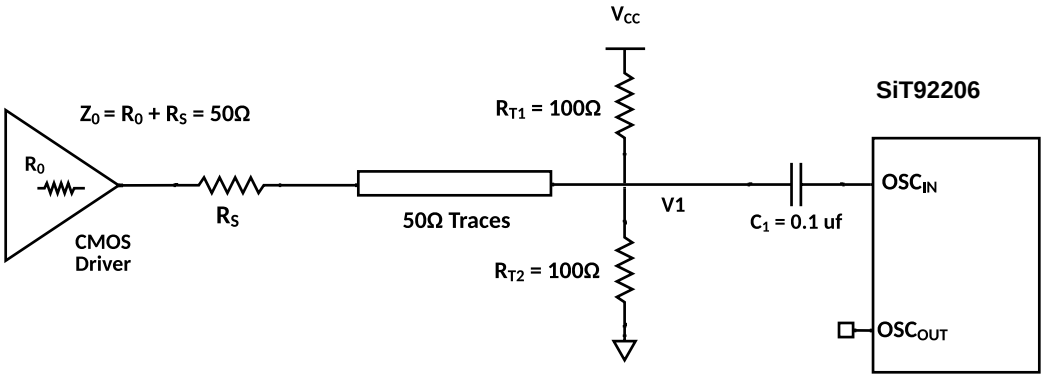


Figure 11. Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 12 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. A 0.1 uF is in series with the CMOS driver to prevent any DC leakage current.

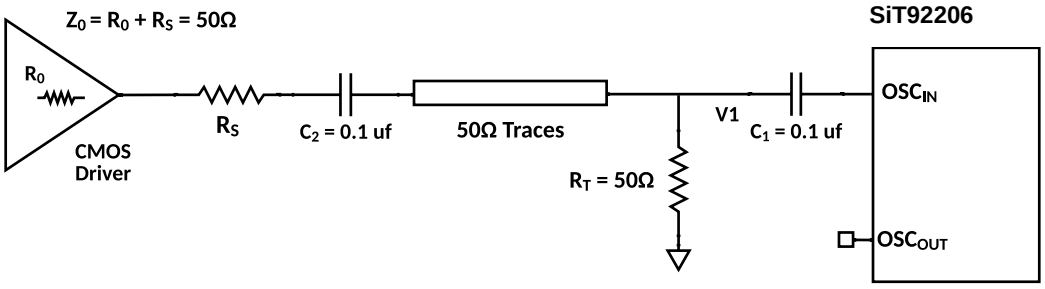


Figure 12. Single ended LVCMOS input – configuration 2, AC coupling to crystal input

Driving OSC_{IN} with LVCMOS Driver (DC coupled)

The crystal input OSC_{IN} can be overdriven with single ended clock as shown in Figure 13, in DC couple mode. The peak swing at OSC_{IN} should be limited to 1.8 V (voltage at the crystal input pin). The OSC_{OUT} pin, in this case can be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.8 V

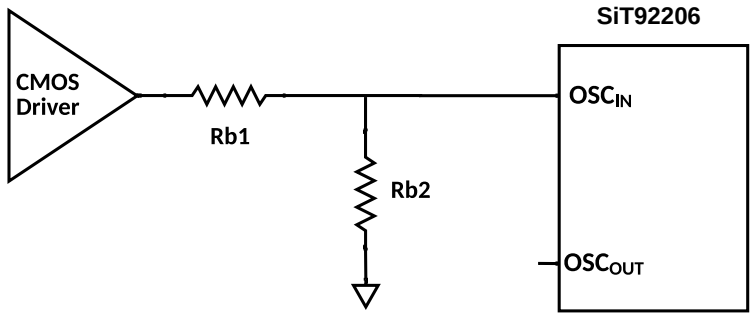


Figure 13. Single ended LVCMOS input, DC coupling to crystal input

LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 14.

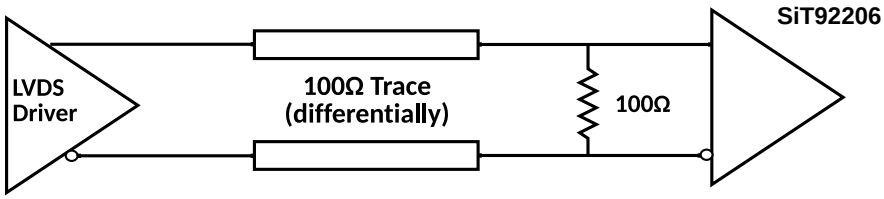


Figure 14. Termination scheme for DC coupled LVDS

HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 15.

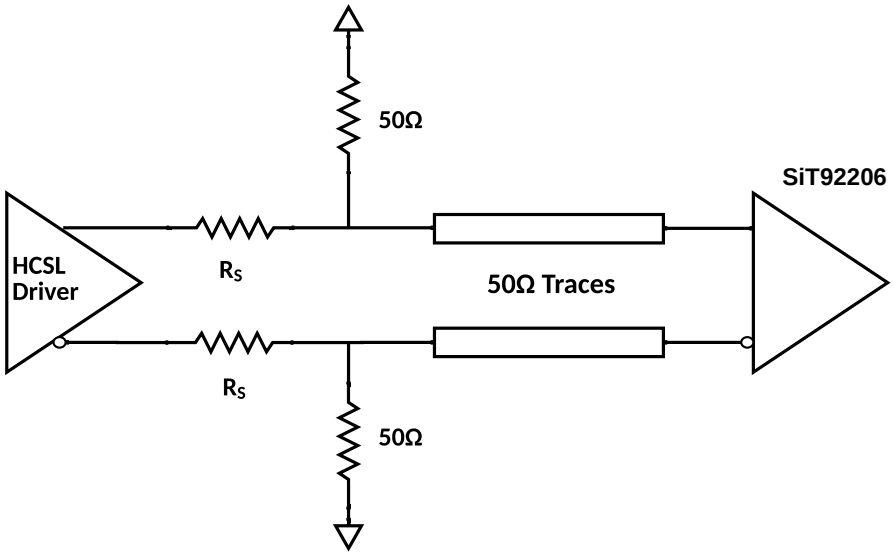


Figure 15. Termination scheme for DC coupled HCSL

LVPECL (DC coupled)

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source VTT.

$$V_{TT} = V_{CCO} - 2V.$$

This termination scheme is shown in Figure 16. Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 17.

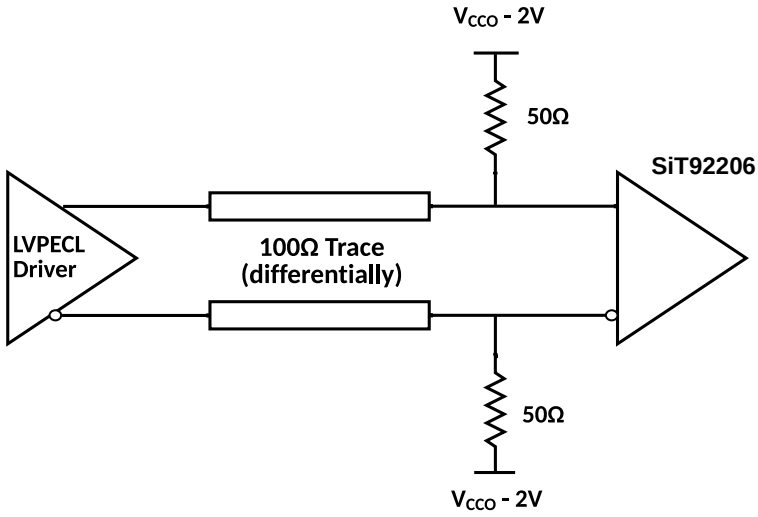
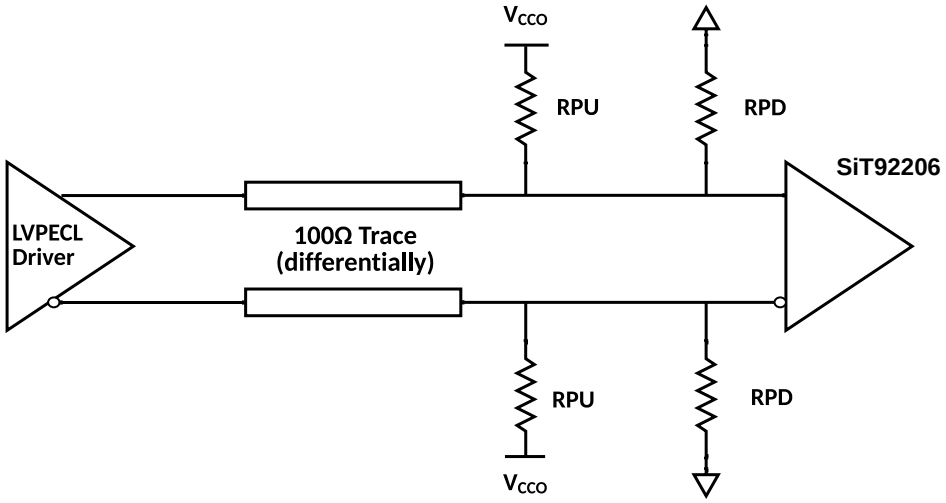


Figure 16. Termination scheme for DC coupled LVPECL



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 17. Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * Vcco}{R_{PD} + R_{PU}} = Vcco - 2V$$

SSTL (DC coupled)

The SSTL input clock configuration is shown in Figure 18. The transmission line impedance is 60 Ω in the application example given. Therefore we use two 120 Ω resistors from V_{CCO} to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω.

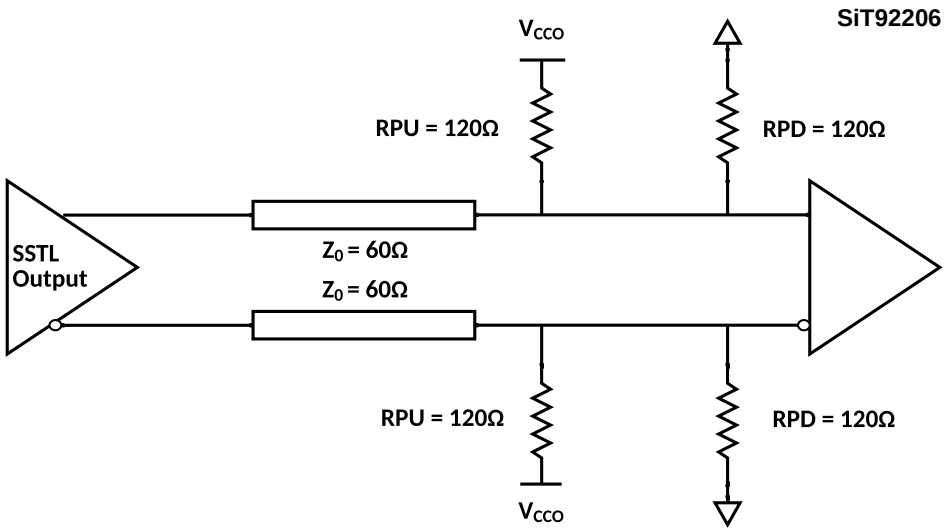


Figure 18. Example of input clock termination for SSTL clock

LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 19.

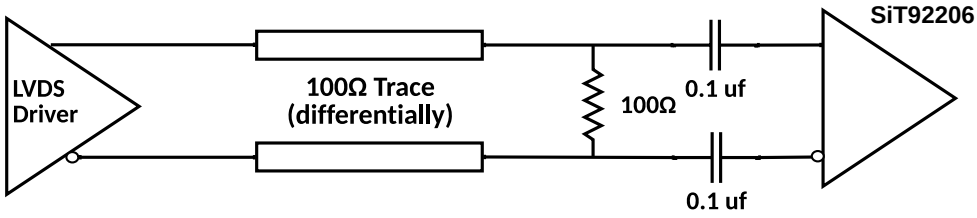


Figure 19. Termination scheme for AC coupled LVDS

LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 20.

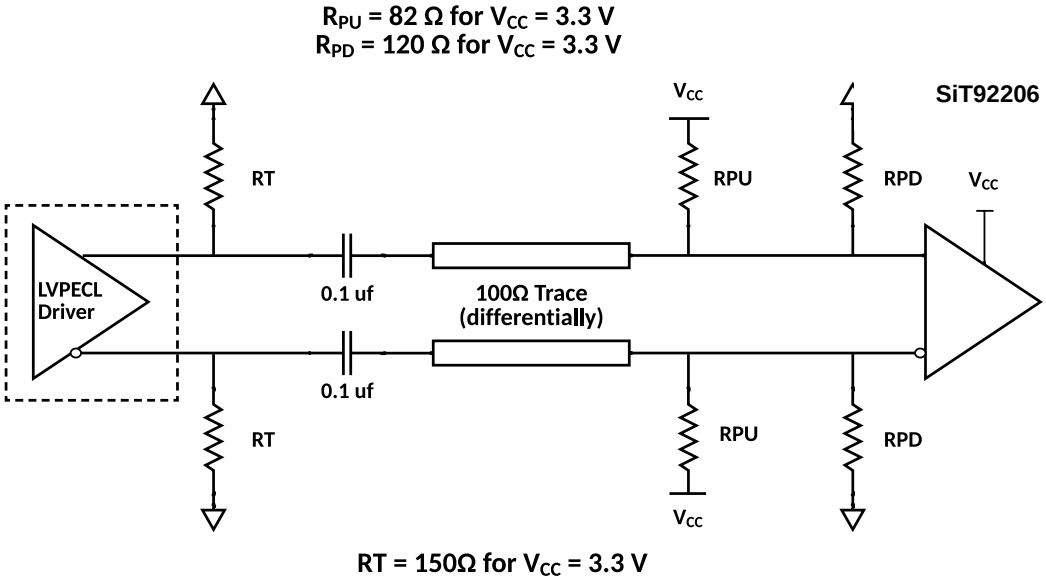


Figure 20. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance RPU and pull down resistance RPD sets the input common mode voltage for SiT92206.
The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{Vcc * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961\,V$$

The differential input common mode specification of SiT92206 (from data sheet) is V_{CC} -1.1 = 2.2 V, therefore the input common mode set by LVPECL AC coupled termination meets the SiT92206 input common mode specification. The LVPECL driver chip has resistance RT providing DC path for the output driver current in the LVPECL driver.
The effective load impedance at the input side of SiT92206 (receiver side) is formed by parallel combination of RPU, RPD.

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\,\Omega$$

Termination of Output Driver of SiT92206 for Various Load Configurations

SiT92206 REF_{OUT} Termination for AC Coupled mode

AC coupling of SiT92206 LVCMOS output driver is shown in Figure 21. We use single termination resistor of 50 Ω to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single 50 Ω resistance to ground. The clock signal is then AC coupled to the receiver, in this example. C1 is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50\ \Omega$$

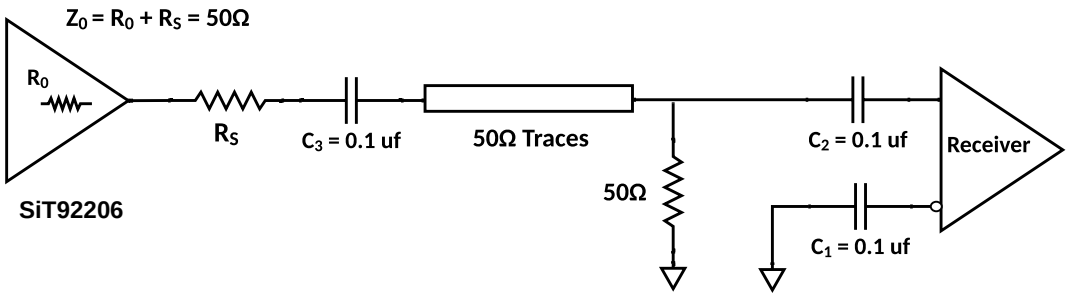


Figure 21. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

SiT92206 REF_{OUT} Termination for DC Coupled mode

Figure 22 shows how SiT92206 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage V1= V_{CC}/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C_1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vcc}{2},$$
$$Typical\ value\ of\ R_{s1} = R_{s2} = 1\ K\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega,$$
$$Typical\ value\ of\ R_{T1} = R_{T2} = 100\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

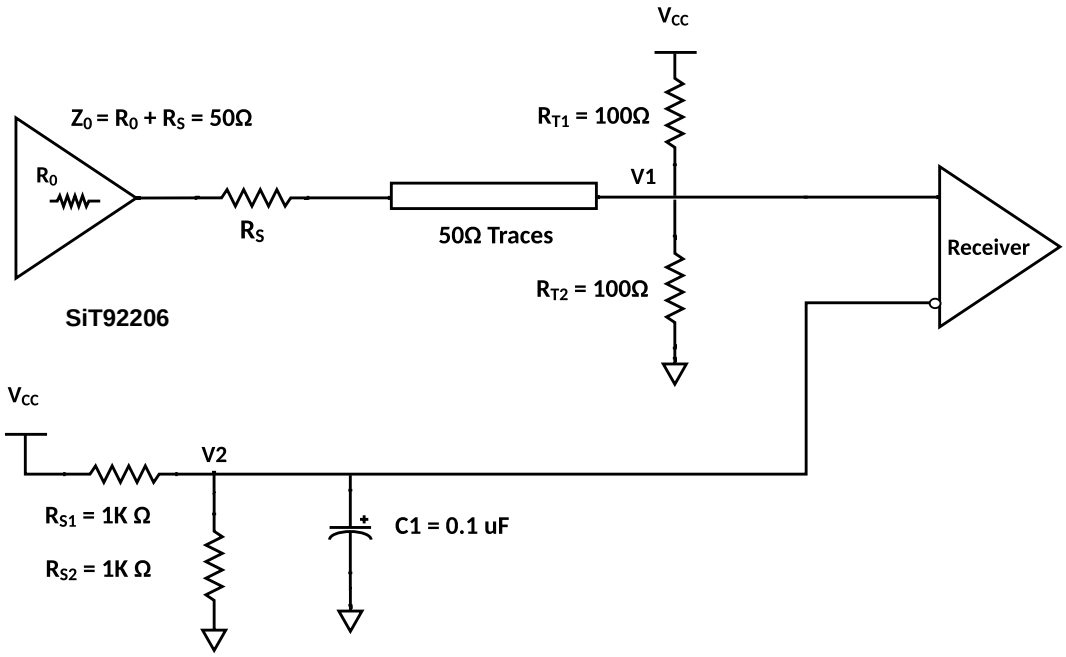


Figure 22. DC coupling of LVCMOS output clock termination – configuration 1

For example, if the SiT92206 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values given below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 23 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. There will be DC leakage current from SiT92206, for the output termination shown in Figure 23. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23 is given below

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2} = \frac{Vcc}{4},$$

$$Typical\ value\ of\ R_{s1} = 3\ K\Omega, R_{s2} = 1\ K\Omega$$

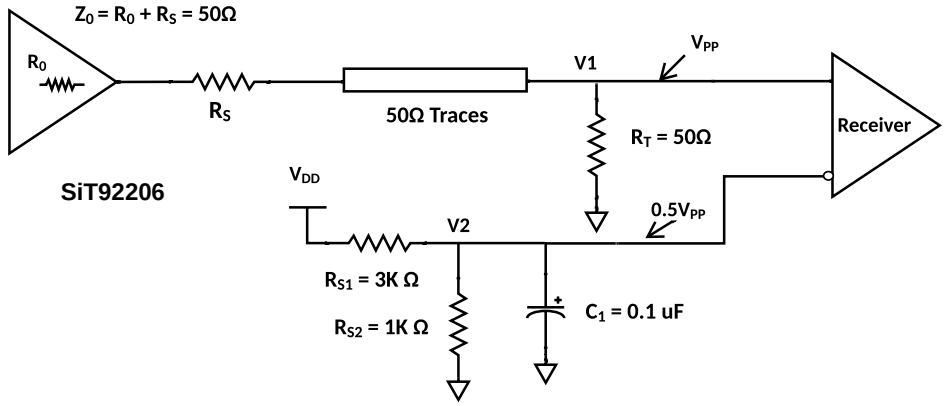


Figure 23. DC coupled LVCMOS output clock configuration – configuration 2

The SiT92206 LVCMOS output driver termination with series RC termination near the buffer is shown in Figure 24. There is a single termination resistor RT which is connected to ground through a capacitor CAC. The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D$$

is the transmission line delay
Typical value for C_{AC} is 60 pF, assuming delay of T_D = 200 ps/inch and 5 inch input clock route length.

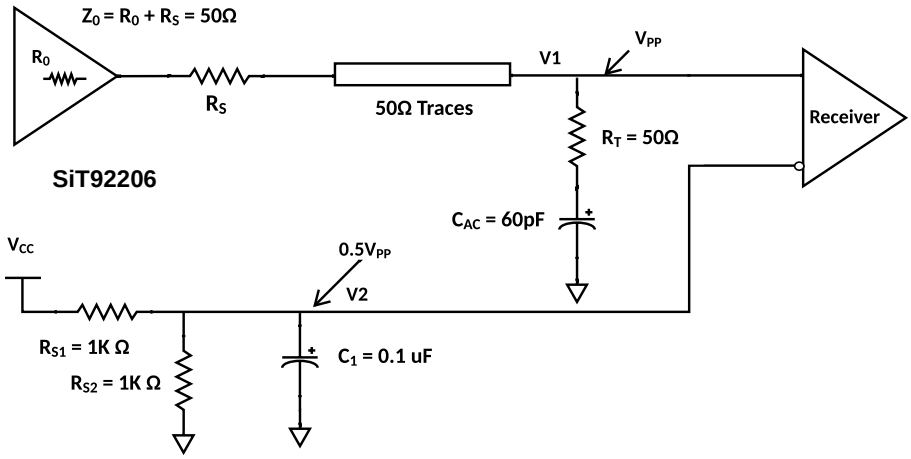


Figure 24. DC coupled LVCMOS output clock with series RC termination – configuration 3

The typical value of R_{S1} and R_{S2} in this case is 1K Ω and that of C_{AC} is 60 pF.

CMOS (Capacitive load)

The capacitive load can be driven as shown in Figure 25 For SiT92206 LVCMOS driver the Ro is very close to 50 Ω by design. Therefore Rs = 0 Ω is recommended.

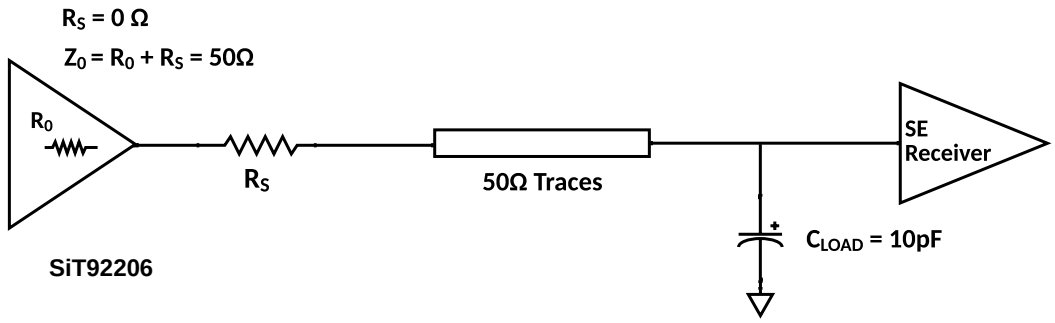


Figure 25. Typical application load

Termination of Output Drivers (DC coupled)

LVDS DC Coupled Output Termination

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 26.

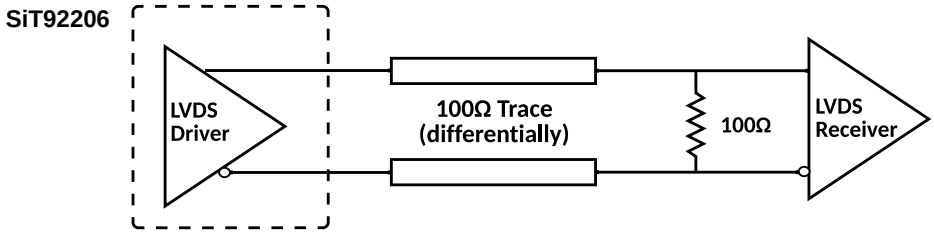


Figure 26. Termination scheme for DC coupled LVDS

HCSL DC Coupled Output Termination

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 27.

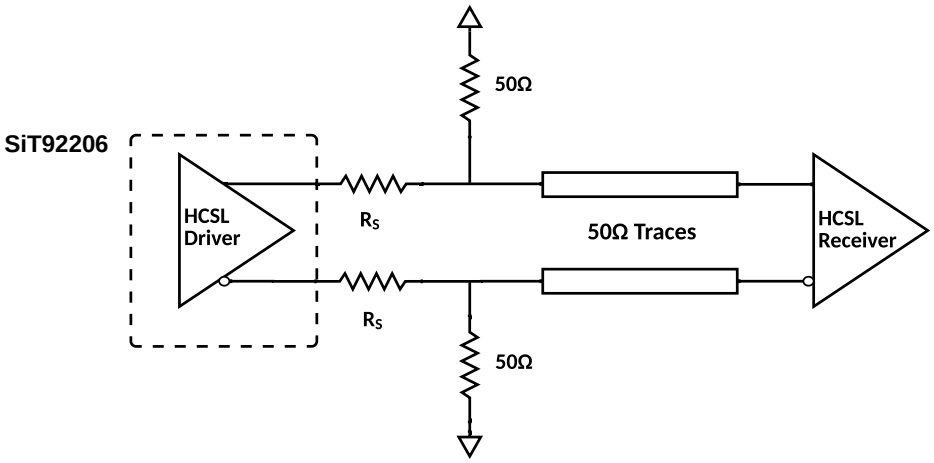


Figure 27. Termination scheme for DC coupled HCSL

LVPECL DC Coupled Output Termination

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source VTT. Typically,

$$V_{TT} = V_{CCO} - 2V.$$

This termination scheme is shown in Figure 28. Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider.

This scheme and the values of the resistors in the resistor divider are given in Figure 29.

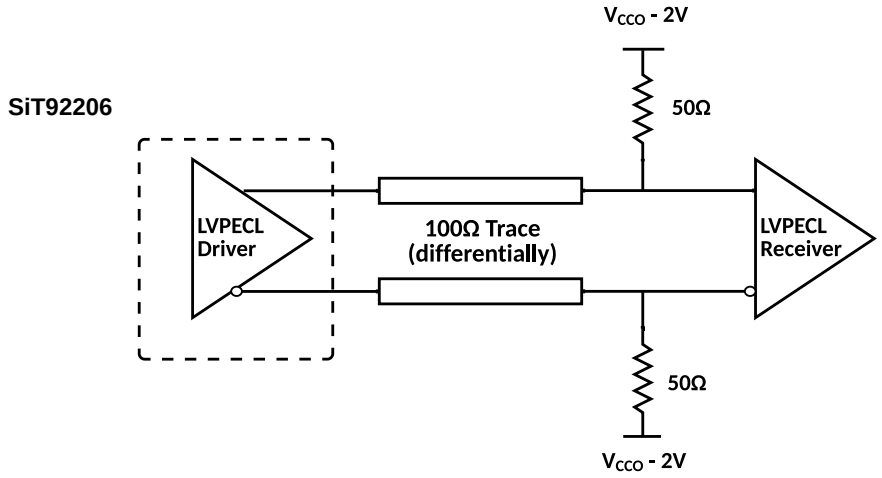
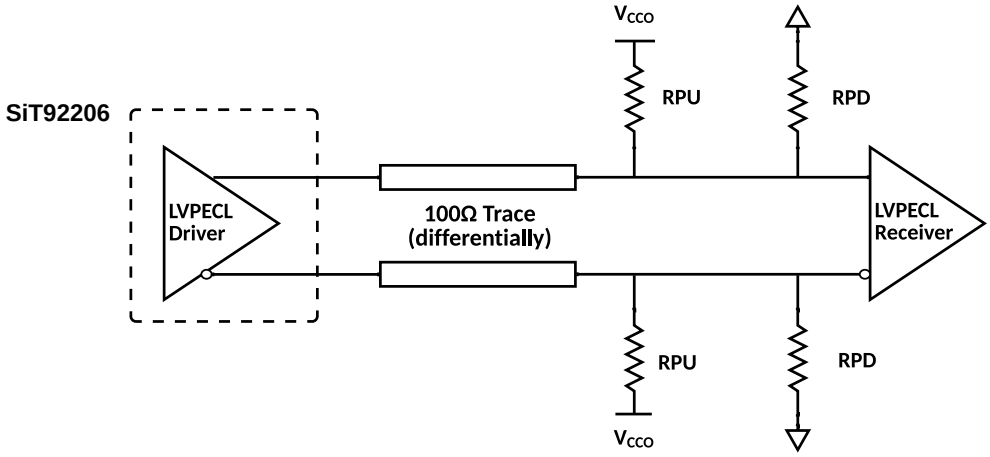


Figure 28. Termination scheme for DC coupled LVPECL

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * Vcco}{R_{PD} + R_{PU}} = Vcco - 2V$$



Vcco	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 29. Termination scheme for DC coupled LVPECL, Thevenin equivalent

Termination of Output Drivers (AC coupled) LVDS AC Coupled Output Termination

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 30. First figure shows SiT92206 output driver configured in LVDS mode. The receiver in this case is shown as LVDS receiver. The second figure shows SiT92206 output driver configured in LVDS mode and the receiver in this case is shown as CML receiver. As long as the LVDS swing is okay with the receiver the AC coupled output termination is same.

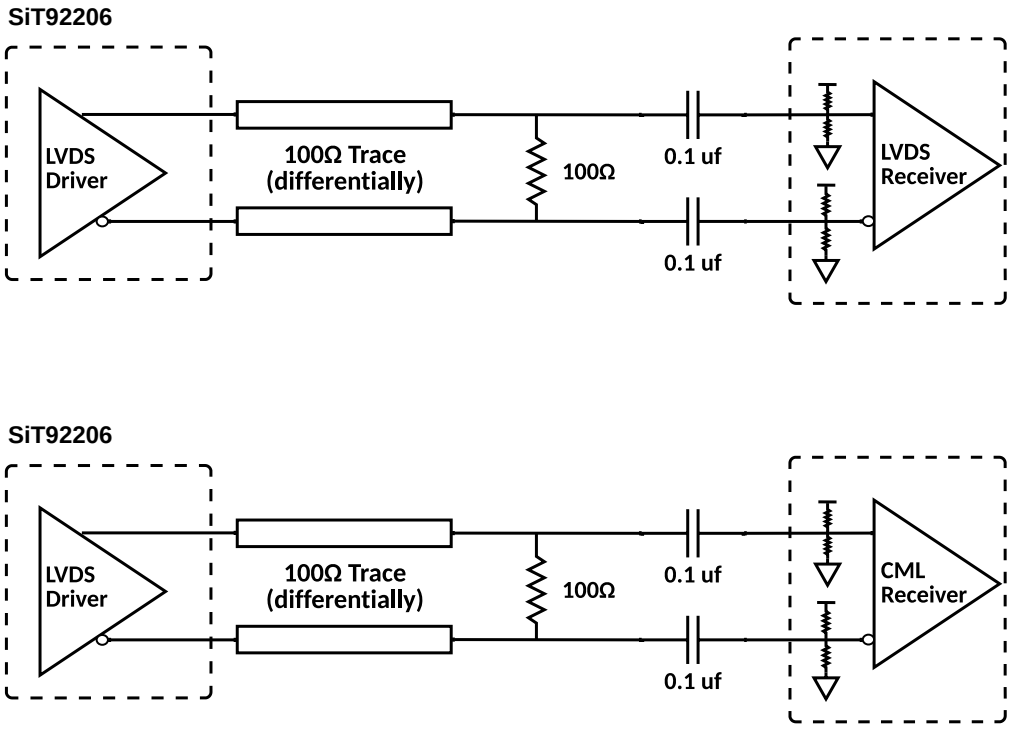


Figure 30. Termination scheme for AC coupled LVDS, driving LVDS receiver and CML receiver

LVPECL AC Coupled Output Termination

The LVPECL should have a DC path to ground. So the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 31. SiT92206 swing reduces by about 20% as the effective load resistor is now the parallel combination of RT at the driver side and 50 Ω at the receiver side.

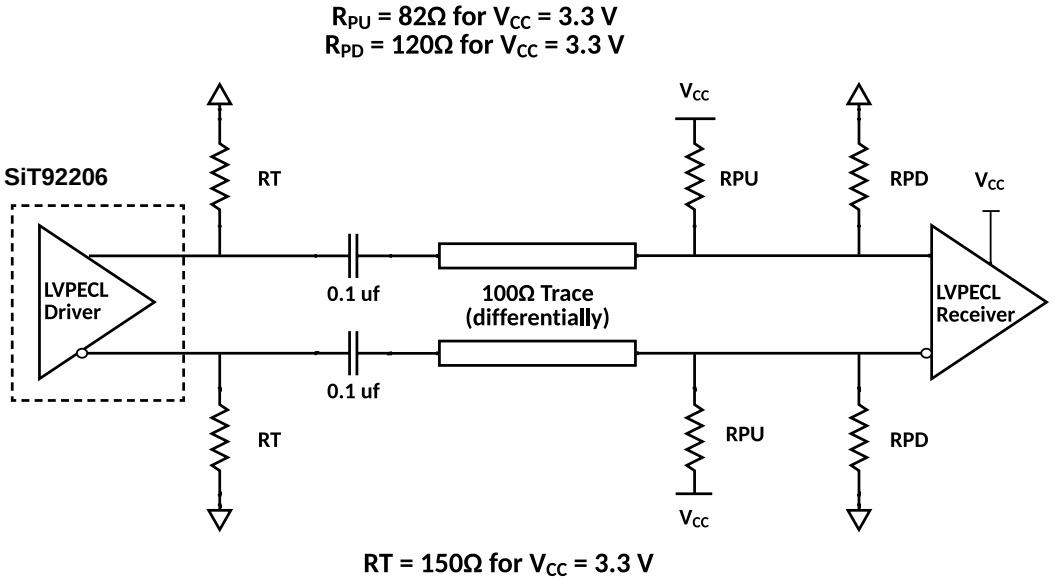


Figure 31. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance RPU and pull down resistance RPD sets the input common mode voltage for LVPECL receiver. The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{Vcc * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The LVPECL driver of SiT92206 has resistance RT providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the receiver side is formed by parallel combination of RPU, RPD. The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

Termination of Output Drivers in LVPECL Mode, Single Ended, DC coupled

Single ended LVPECL operation is possible. The user can use a balun to convert differential output to single ended output. It is also possible to use the LVPECL driver as one or two separate 700 mV - PP signal. The unused output need to be terminated close to the output driver.

These termination schemes are shown in Figure 32 and Figure 33.

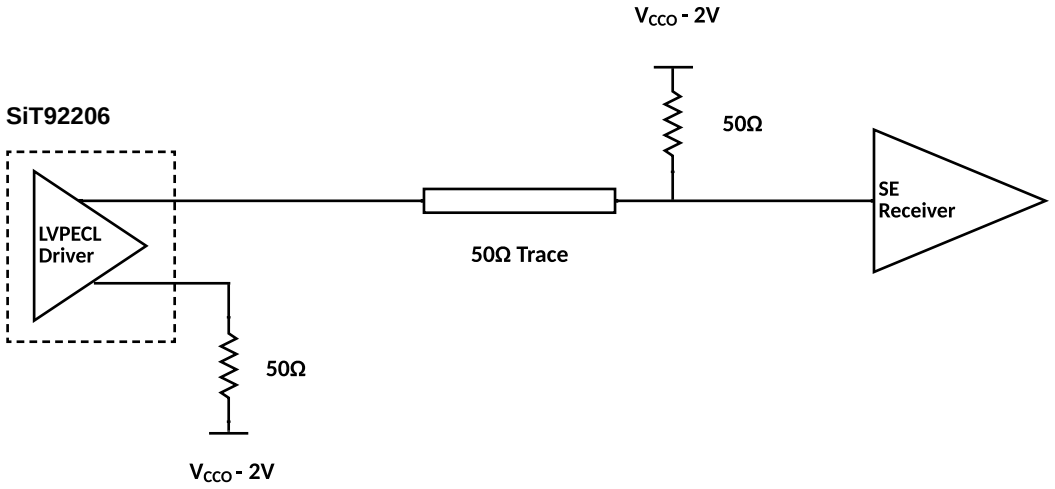
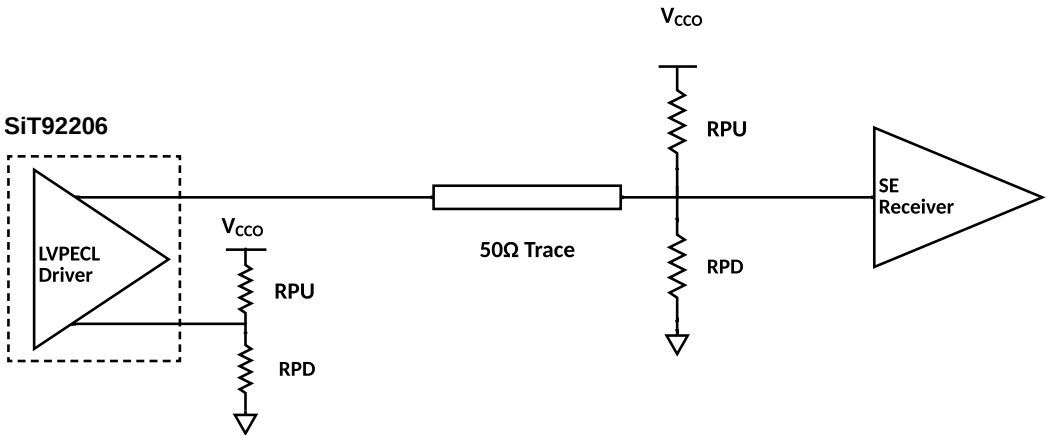


Figure 32. Termination scheme for DC coupled LVPECL, single ended

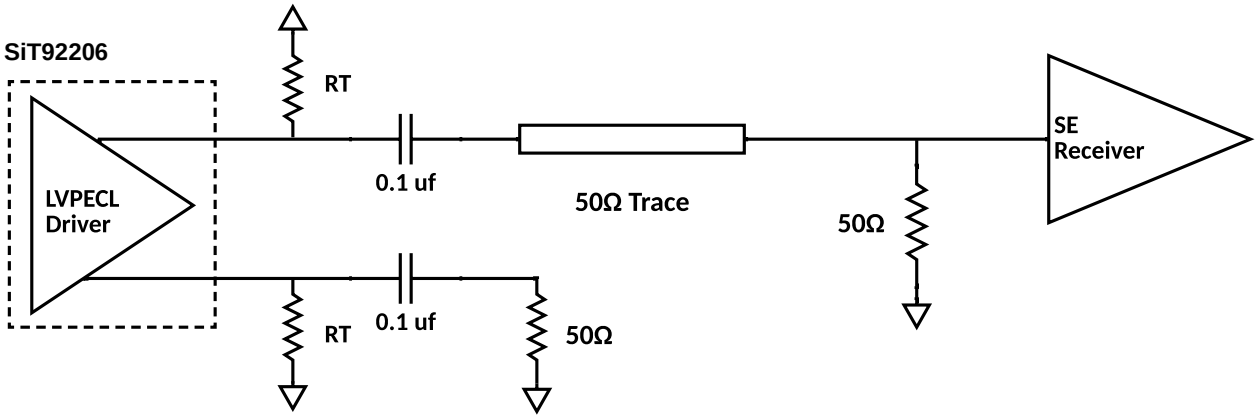


V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 33. Termination scheme for DC coupled LVPECL, single ended, Thevenin equivalent

Termination of Output Drivers in LVPECL Mode, Single Ended, AC coupled

LVPECL output driver needs a DC path to ground from its output. Therefore 160 Ω (if V_{CC} = 3.3 V) resistor to ground is connected from the output of the LVPECL driver to ground. If V_{CC} = 2.5 V, the DC path resistance should be 91 Ω. The 50 Ω load termination resistor must be placed close to input receiver and biased to a suitable voltage.



V_{CCO}	RT
3.3 V	160 Ω
2.5 V	91 Ω

Figure 34. Termination scheme for AC coupled LVPECL, single ended

Termination of Output Drivers in AC coupled HCSL mode

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. AC coupling capacitor of 0.1 uF is used to couple the output HCSL signal in to the receiver. The same termination can be used for CML receiver.

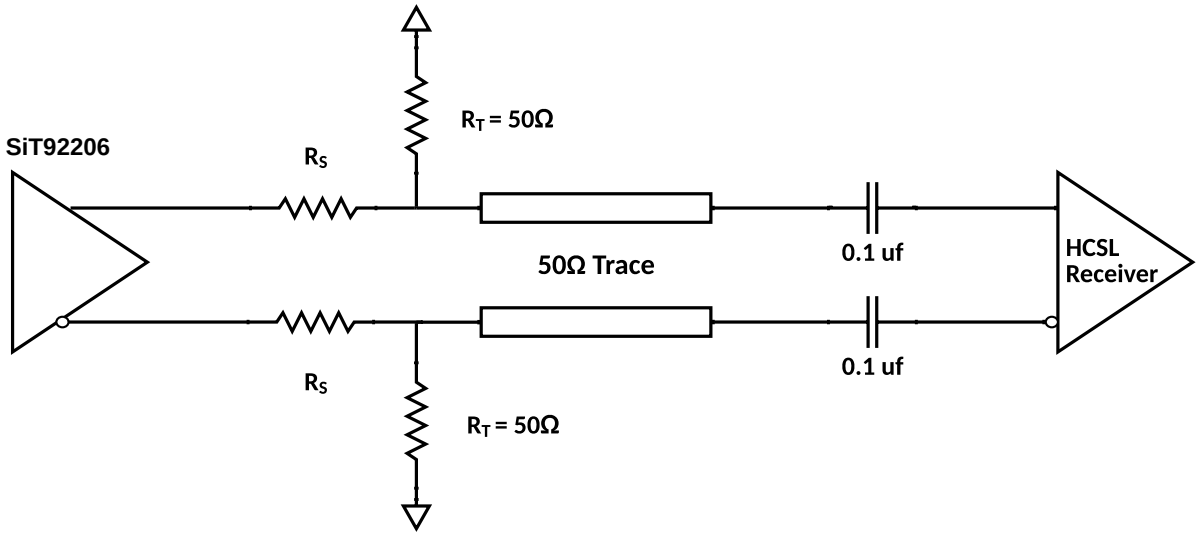


Figure 35. Output driver termination in HCSL AC coupled mode

Thermal Metrics

Table 16. Thermal Metrics

Thermal Metric	SiT92206 QFN 36 pins	Units
θ_{JA} Junction to ambient thermal resistance	33.1	°C/W
θ_{JB} Junction to board	3.60	°C/W
θ_{JC} Junction to case	29.6	°C/W
ψ_{JT} Junction to top characterization parameter	0.43	°C/W

HOT Swap Recommendations

Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

Typical Differential Input Clock

For example, Figure 36 shows a typical LVPECL driver and differential input. If the power of the driver (V_{CCO}) is turned on before the input supply (V_{CCI}), there is a possibility that the input current could exceed the limit and damage diode D1.

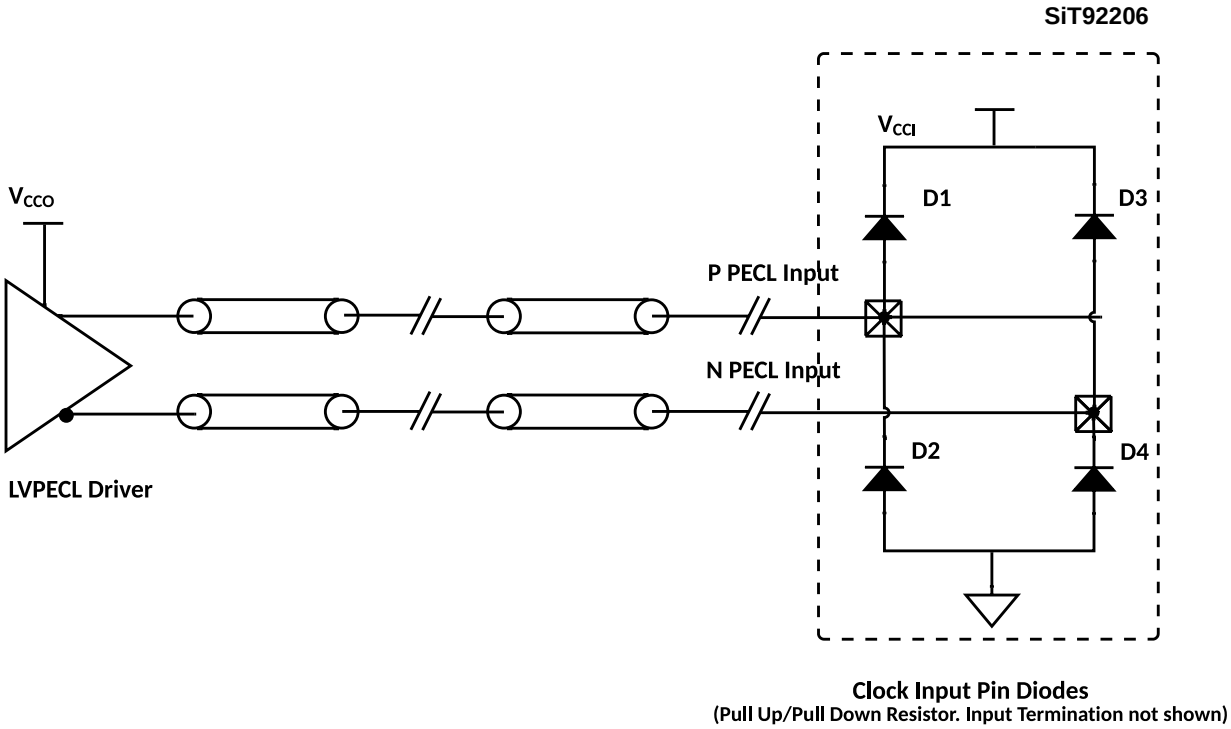


Figure 36. Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the examples have an optional 100 pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

Input Clock Termination with Hot Swap Protection

LVPECL Termination Example

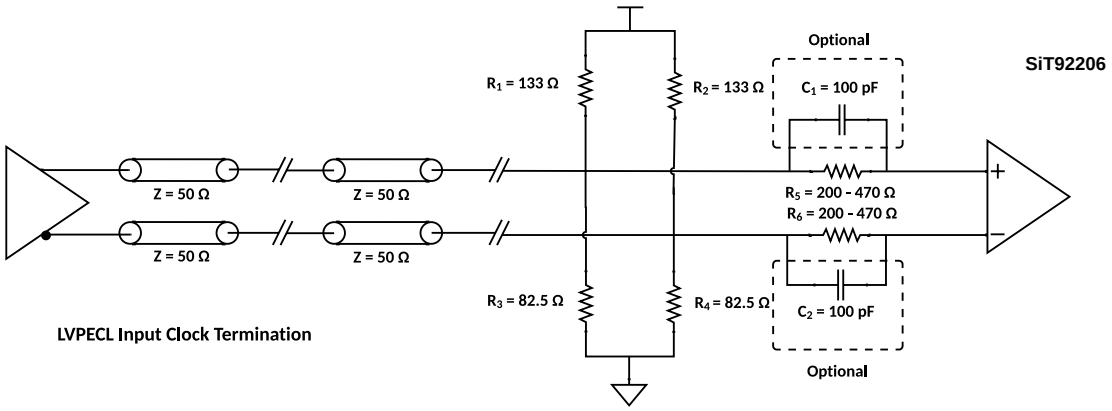


Figure 37. LVEPCL termination with hot swap protection

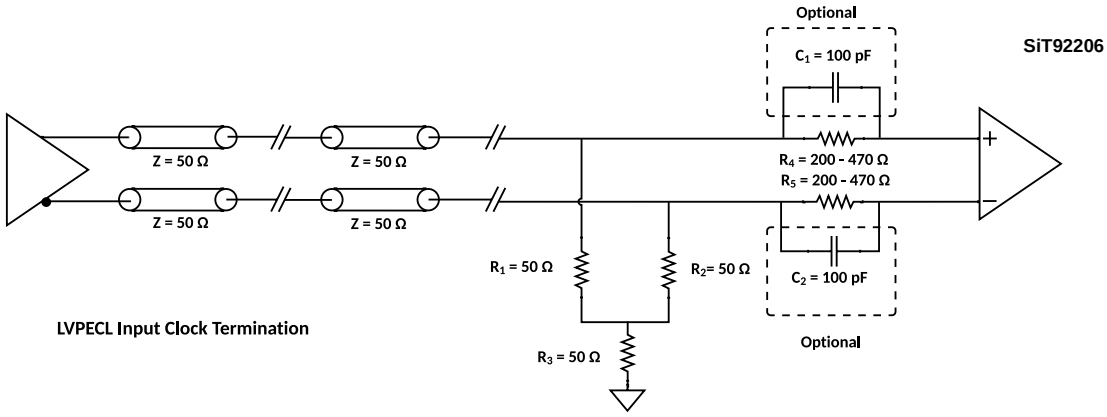


Figure 38. LVPECL termination with hot swap protection

LVDS Input Clock Termination Example

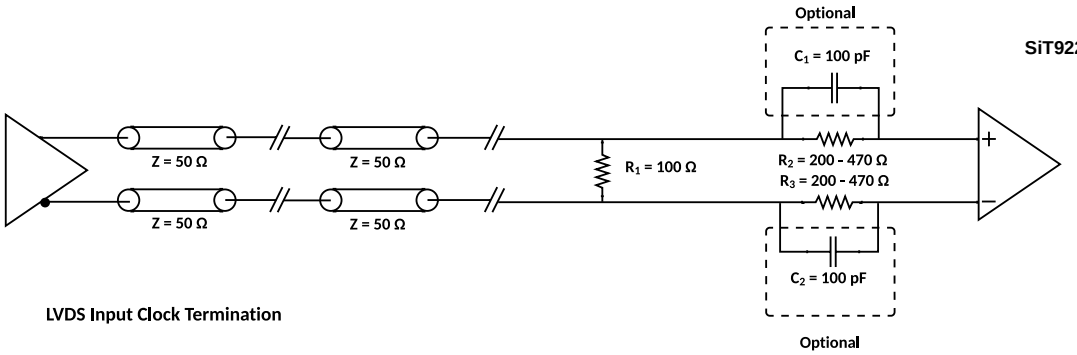


Figure 39. LVDS termination with hot swap protection

HCSL Input Clock Termination Example

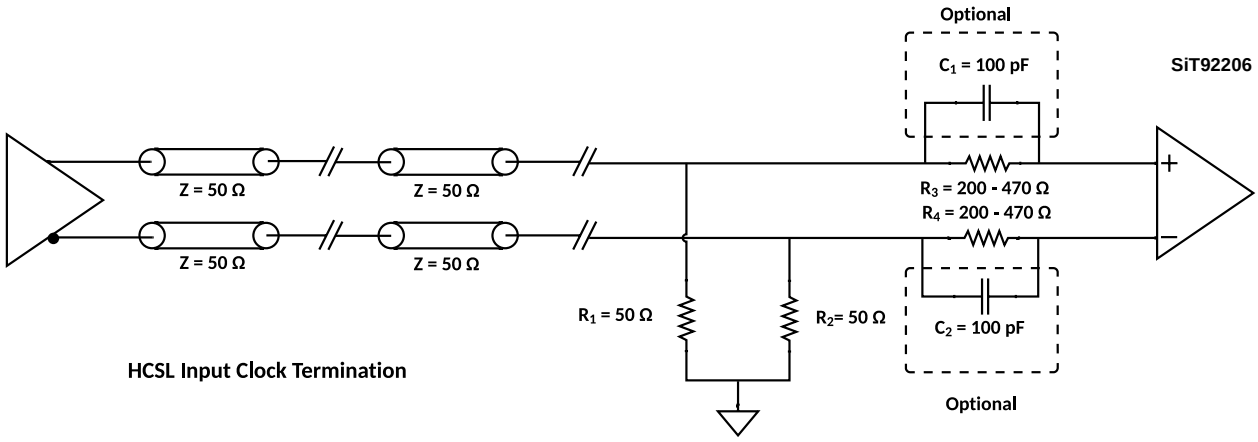


Figure 40. HCSL termination with hot swap protection

LVCMOS Input Clock Termination with Hot Swap Protection

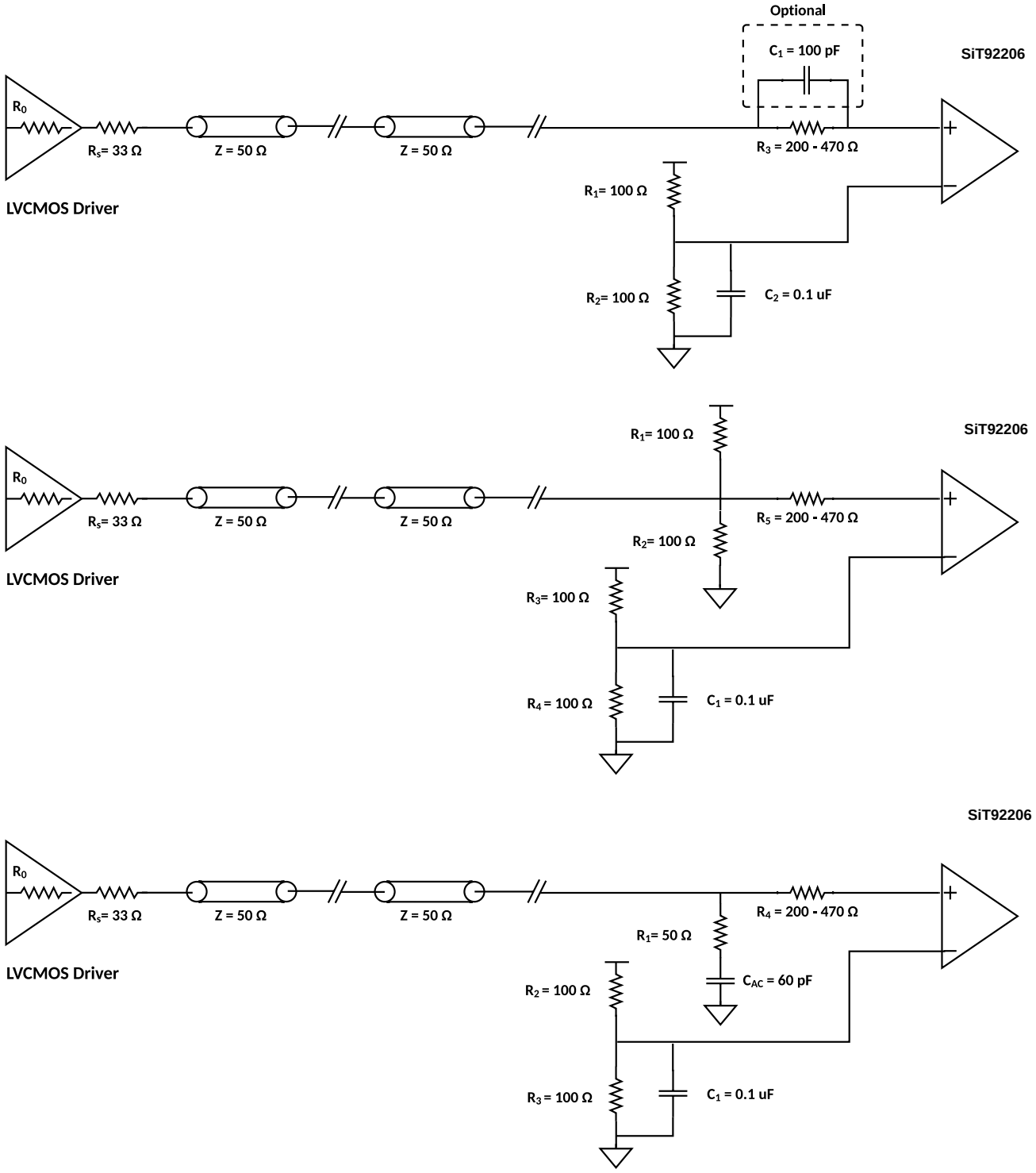


Figure 41. LVCMOS input clock termination with hot swap protection

LVCMOS Output Clock Termination with Hot Swap Protection

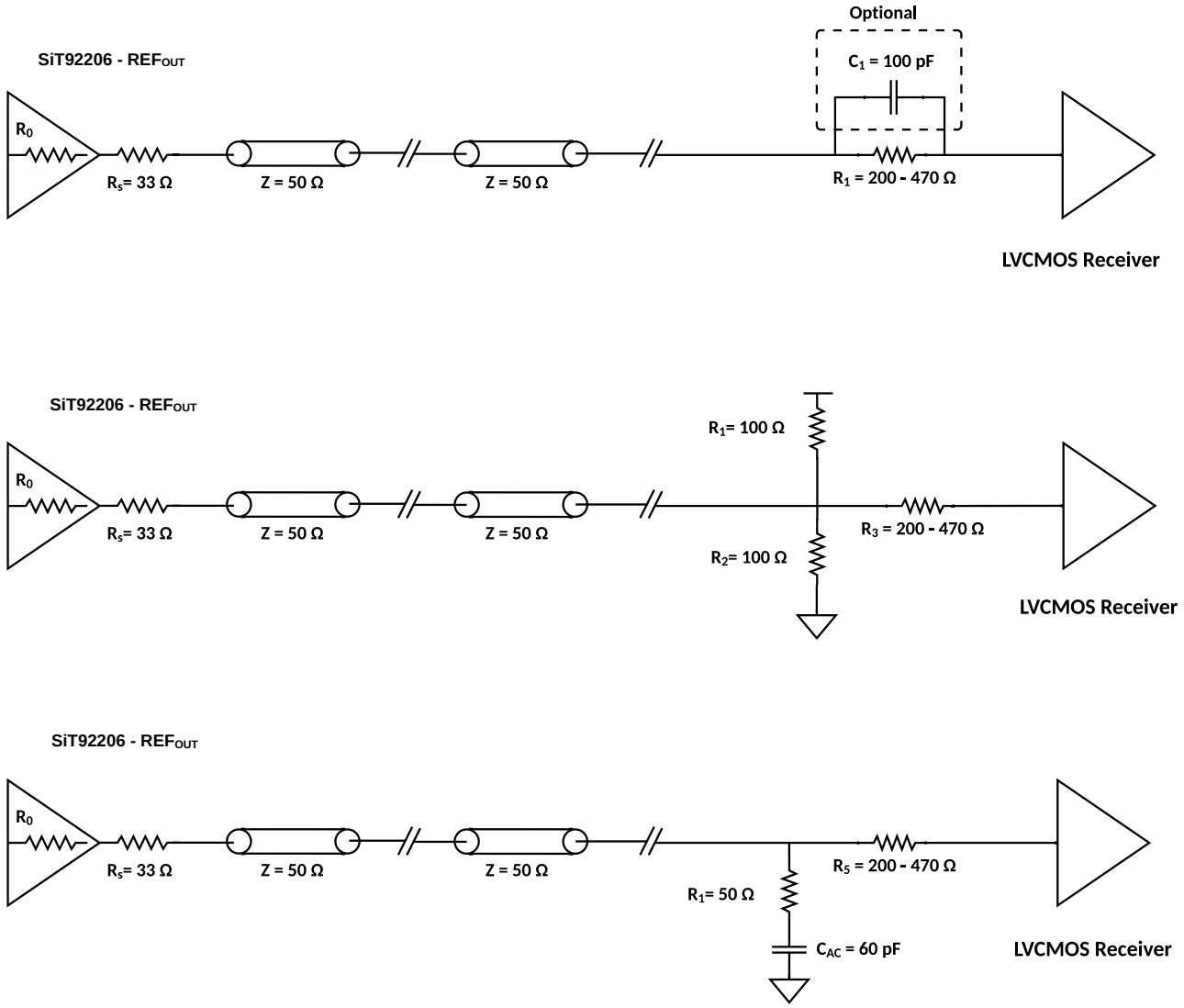


Figure 42. Different types of LVCMOS output clock termination with hot swap protection.

Parameter Measurement Information

Differential Input Level

The parameter definitions related to differential input level is shown in Figure 43.

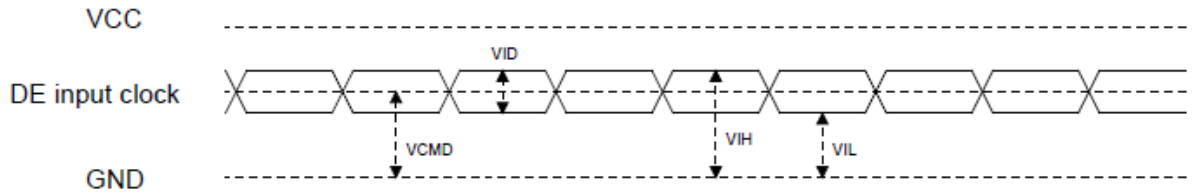


Figure 43. Parameters related to differential input level

Differential Output Level

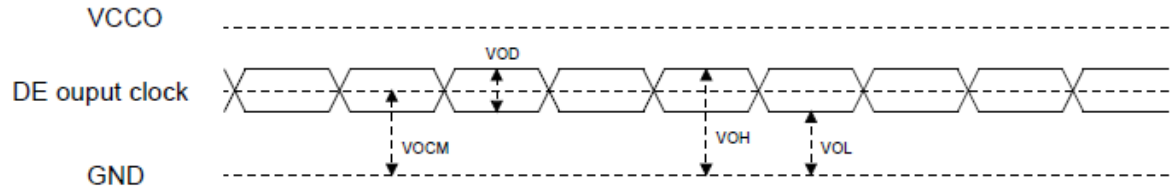


Figure 44. Parameters related to differential output clock levels

Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown in Figure 45.

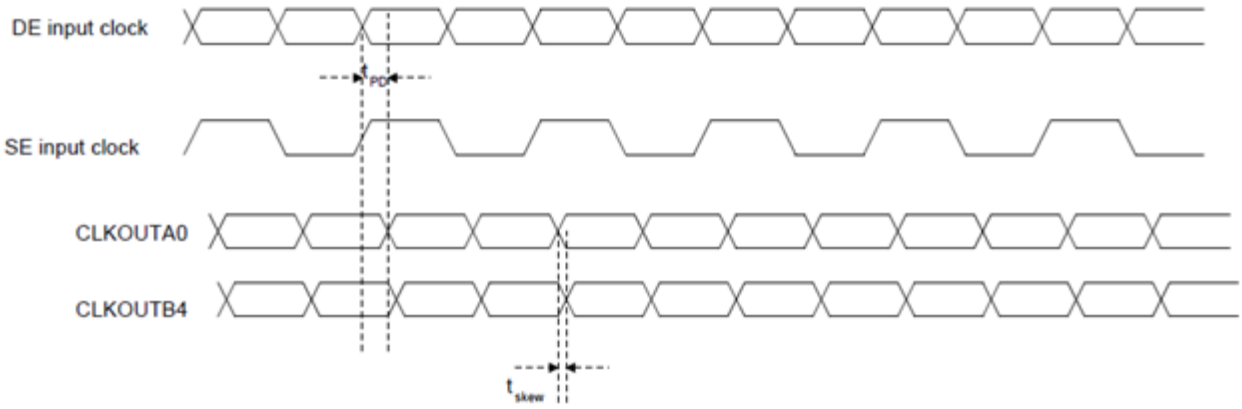


Figure 45. Parameter definitions of propagation delay and skew

Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown in Figure 46.

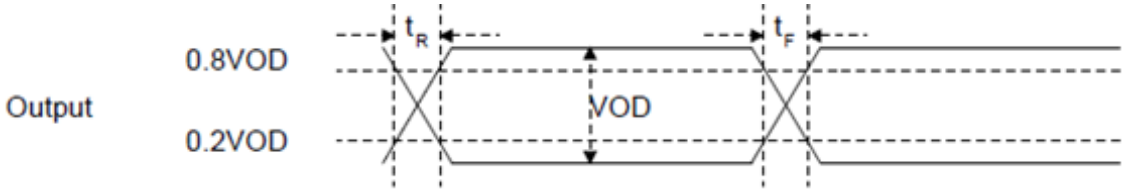


Figure 46. Parameter definitions related to rise and fall times

Isolation

Isolation is a measure of the coupling of clock toggling in unselected input clock path on the output clock. Let us say that CLOCK0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in CLOCK1 path at 156 MHz at 0 dBm, then we there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

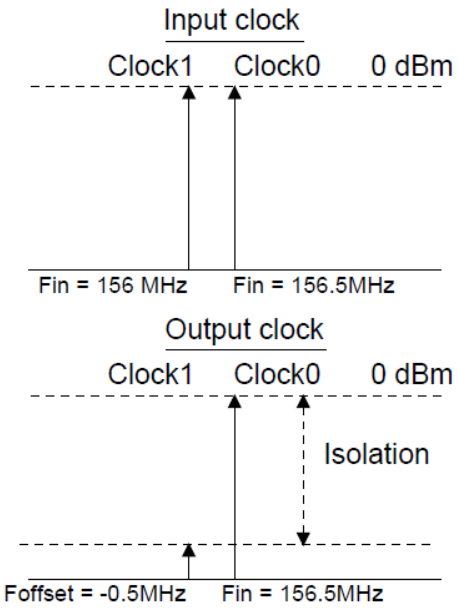


Figure 47. Parameter definition of isolation

Operation in Multiple V_{CCO} Supply Domains

The V_{CCOA} pins, 2 and 5 on the left side are shorted internally. These pins along with ODR $CLK_{OUT}A0$ to $CLK_{OUT}A2$ belong to a single supply domain. The VCCOB pins, 27 and 24 on the right side are shorted internally. These pins along with ODR $CLK_{OUT}B0$ to $CLK_{OUT}2$ belong to a single supply domain. These two supply domains are totally independent of each other. Pin 2, 5 can be connected to say 3.3 V while pin 27, 24 can be connected to 2.5 V. In this example, $CLK_{OUT}A0$ to $CLK_{OUT}A2$ will be 3.3 V output driver. $CLK_{OUT}B0$ to $CLK_{OUT}B2$ will be 2.5 V output driver.

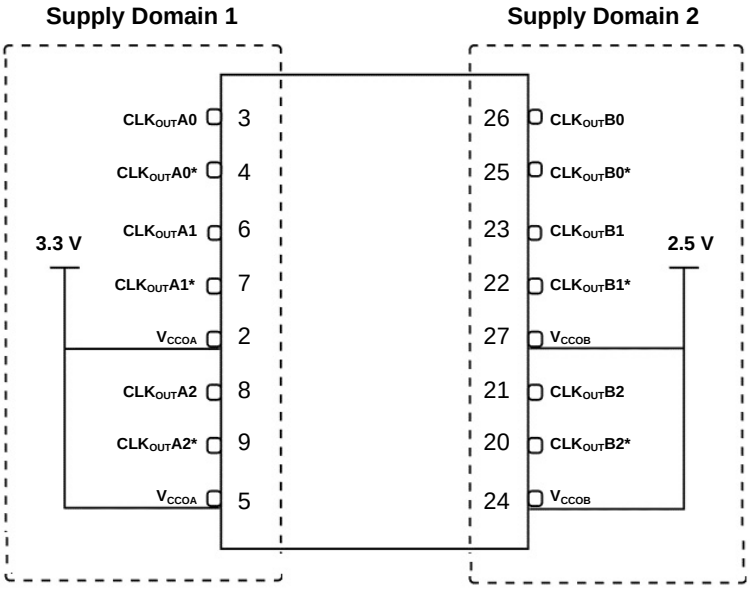
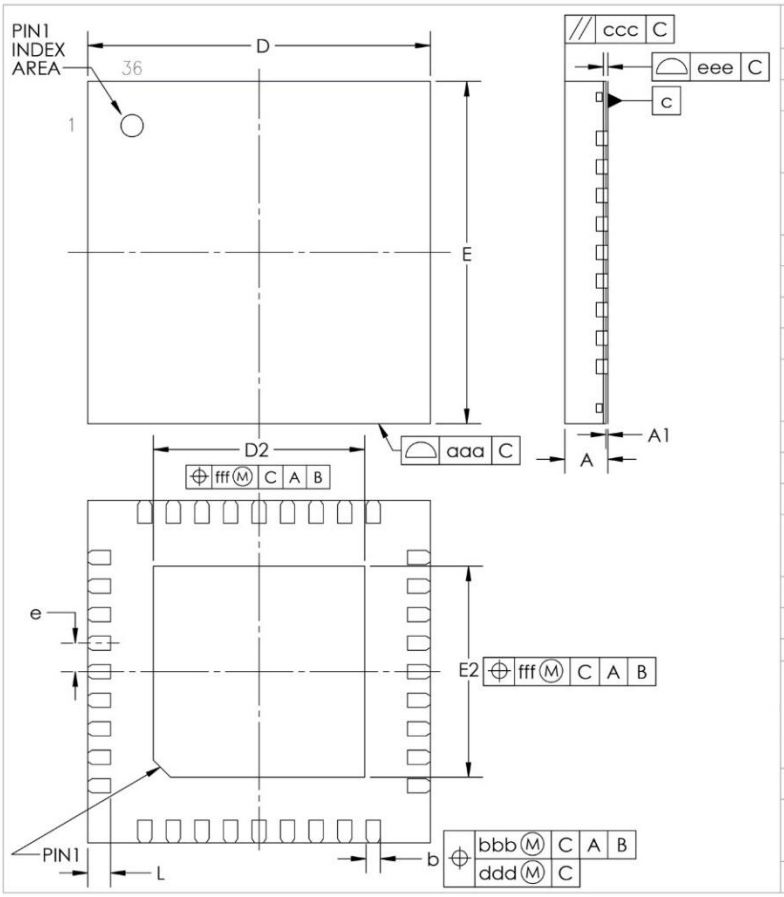


Figure 48. Multi Supply operation of SiT92206

Package Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



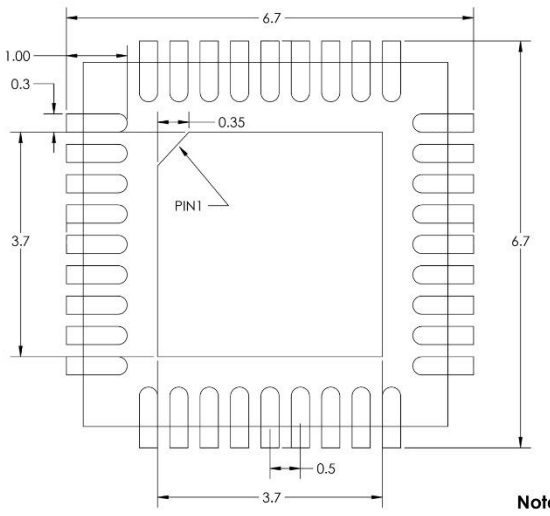
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	0.035	0.05
BODY SIZE	X	D		6.00 BSC	
	Y	E		6.00 BSC	
EXPOSED PAD	X	D2	3.60	3.70	3.80
	Y	E2	3.60	3.70	3.80
LEAD PITCH		e		0.50 BSC	
LEAD WIDTH		b	0.20	0.25	0.30
LEAD LENGTH		L	0.30	0.40	0.50
PACKAGE TOLERANCE		aaa		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
EXPOSED PAD OFFSET		fff		0.1	

NOTE

1. ALL DIMENSIONS IN MM

PKG INFO		DRAWING NO.	
36L PQFN 6.00X6.00X0.75 mm		POD-098-PQFN-036-C06060	
		REV	SHEET
DATE	04/05/2024	A01	1 fo 1

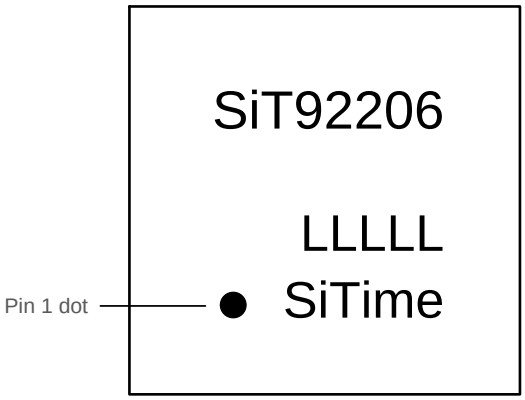
Recommended Land Pattern (Unit: mm)



Note: All units in mm.

	PKG INFO	SPL DRAWING NO.	
		SPL-098-PQFN-036-C06060	
DATE	36L PQFN 6.0X6.0 mm	REV	SHEET
04/05/2024		A01	1 of 1

Top Marking



Line 1: “SiT92206”, SiTime part number
Line 2: Blank
Line 3: “LLLLL”, Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo

Thermal Management

SiT92206 has an exposed pad (EPAD) on the package to provide the means for thermal relief and excellent grounding. A land pattern must be incorporated on the circuit board as detailed in the package drawing; additional guidelines listed below:

- Minimal number of thermal vias: 9
- Minimal plating thickness of thermal vias: 25 µm
- Minimal thermal via diameter: 0.3 mm (can be smaller for larger number of vias)
- Minimal combined thickness of ground plane(s): 35 µm (1 oz)
- Thermal vias should be directly under the EPAD
- Thermal vias should be through holes
- Thermal vias should be connected around their entire circumference with all ground plane(s)
- Essentially, it is recommended to have a board design that has equal or better thermal dissipation than the JESD51-5 board

Revision History

Table 17. Revision History

Revisions	Release Date	Change Summary
0.5	15-Apr-2024	Initial Release
0.51	23-May-2024	Corrected pin functions for #22 and #23 in Figure 2, Table 10 and Figure 48
0.52	8-Jul-2024	Ordering Information update
0.53	28-Mar-2025	Ordering Code for Packaging updated with 4Ku/reel code “P” and 500u/reel code “N” Added Top Marking section

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