SiT5376 10 MHz – 60 MHz, ±0.1 to ±0.25 ppm, Elite RF™ Precision Super-TCXO

ADVANCED

Description

The SiT5376 is a ±100 ppb precision MEMS Super-TCXO designed for the RF market, ideally suited for high-reliability wireless, telecom, microwave, satellite, radar, and GNSS applications.

The SiT5376 combines SiTime's MEMS technology with a low-noise digital PLL to deliver:

- RF-quality phase noise,
- Excellent dynamic stability in the presence of airflow and thermal excursions,
- Extreme resistance to shock and vibration.

Multiple on-chip regulators are included to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT5376 offers two device configurations for:

1) TCXO with non-pullable output frequency,
2) DCTCXO enabling digital pulling of output frequency via an I²C/SPI interface with a resolution of 0.05 ppt (parts per trillion).

The SiT5376 can be factory programmed for frequency, stability, voltage, and pull range, eliminating long lead times and customization costs associated with quartz devices. Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations.

Features

- Any frequency from 10 MHz to 60 MHz (refer to SiT5377 for 60 MHz to 220 MHz)
- Factory programmable options for short lead time
- Best dynamic stability under airflow, thermal shock
  - ±100 ppb stability across temperature
  - ±1 ppb/°C typical frequency slope (dF/dT)
  - 1e-11 ADEV at 10 seconds averaging time
- -40°C to +105°C operating temperature
- No activity dips or micro jumps
- Resistant to shock, vibration, and board bending
- On-chip regulators eliminate the need for external LDOs
- Digital frequency pulling (DCTCXO) via I²C/SPI
  - Digital control of output frequency and pull range
  - Up to ±400 ppm pull range
  - Frequency pull resolution down to 0.05 ppt (5e-14)
- 1.8 V to 3.3 V supply voltage
- Regulated LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free
- Contact SiTime for voltage control option

Applications

- 4G and 5G radios
- Macro and small cell base stations
- IEEE 1588 (PTP) boundary and grandmaster clocks
- RF upconverters and downconverters
- Reference for jitter cleaners driving RF signal chains
- Radar, satellite, microwave equipment
- WiFi equipment
- Cable infrastructure
- GPS, GNSS systems
- Instrumentation, test, and measurement equipment

Block Diagram

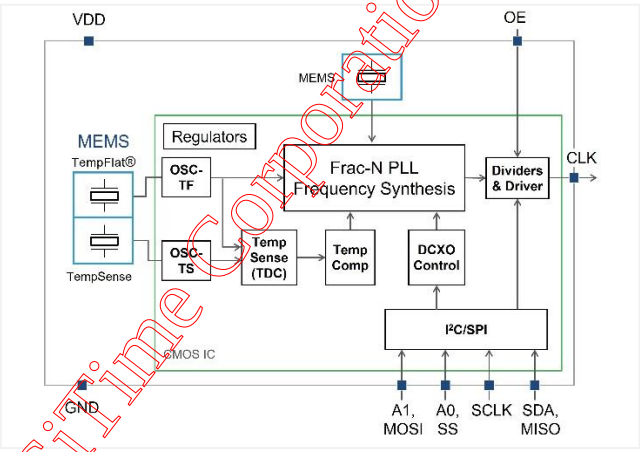


Figure 1. SiT5376 Block Diagram

5.0 mm x 3.5 mm Package Pinout

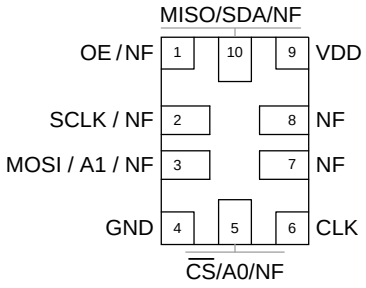
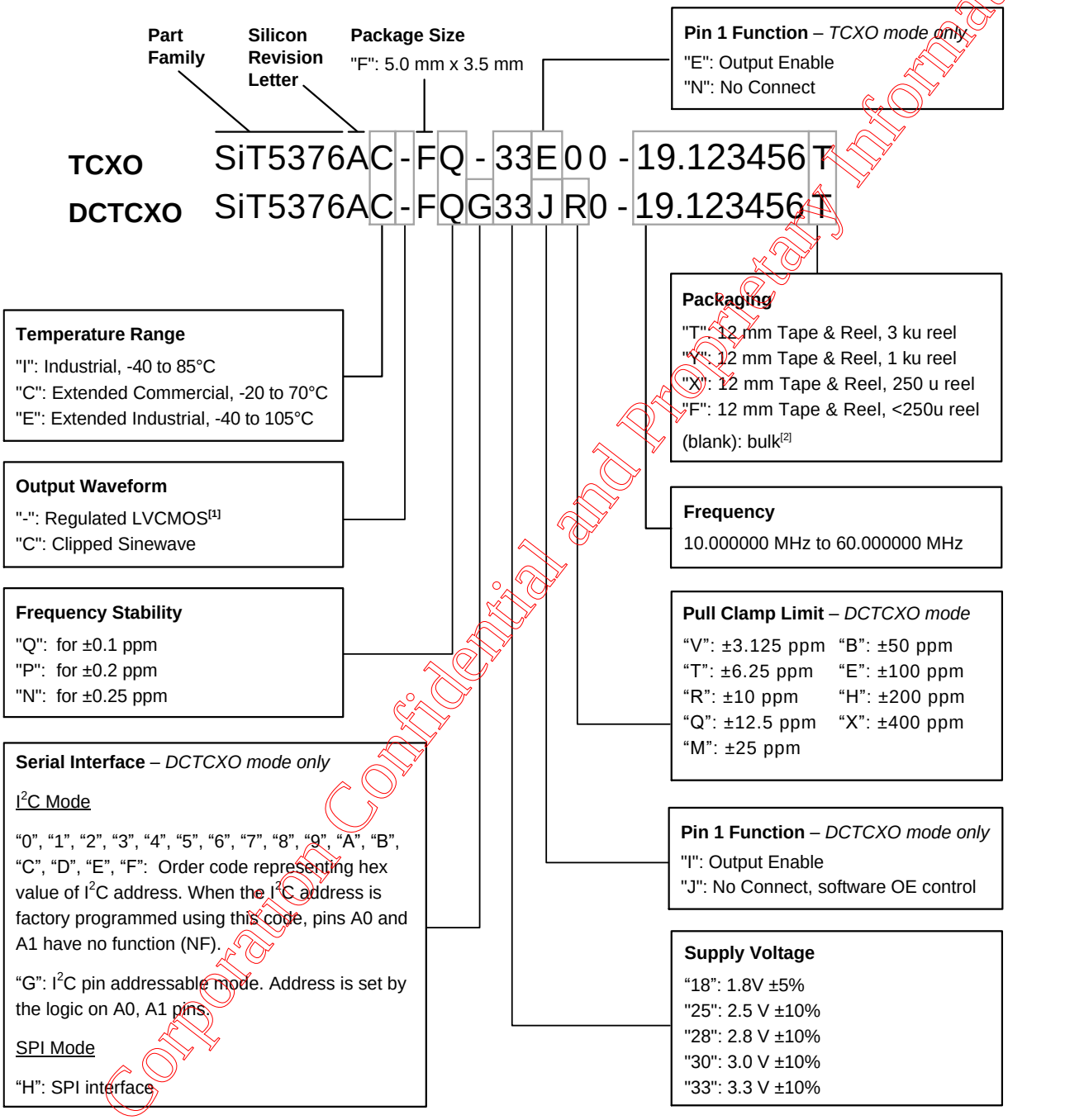


Figure 2. Pin Assignments (Top view)
(Refer to Table 11 for Pin Descriptions)

Ordering Information

The part number guide illustrated below is for reference only, in which boxes identify order codes having more than one option.



Notes:

1. "-" corresponds to the default rise/fall time for Regulated LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, contact SiTime.
2. Bulk is available for sampling only.

TABLE OF CONTENTS

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 8 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	10	–	60	MHz	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+105	°C	Extended Industrial, ambient temperature
Frequency Stability – Stratum 3+ Grade						
Frequency Stability over Temperature	F_stab	–	–	±0.1	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range, in TCXO or DCTCXO Contact SiTime for ±50 ppb frequency stability over temperature
Initial Tolerance	F_init	–	–	±0.3	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±2.5	–	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±0.4	–	ppb	Regulated LVCMOS output, 8 pF ±10%. Clipped sinewave output, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	dF/dT	–	±0.9	–	ppb/°C	1°C/min temperature ramp rate
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.015	–	ppb/s	1°C/min temperature ramp rate
24-hour holdover stability	F_24_Hold	–	–	±0.15	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±0.8 pF load variation and 24-hour aging
Hysteresis Over Temperature	F_hys	–	±10	–	ppb	1°C/min ramp rate, defined as ±dF/2 as shown in Figure 16
One-Day Aging	F_1d	–	±0.25	–	ppb	At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±40	–	ppb	At 50°C, after 2-days of continued operation. Aging is measured with respect to day 3
10-Year Aging	F_10y	–	±50	±500	ppb	
20-Year Aging	F_20y	–	±70	–	ppb	
Allan deviation	ADEV	–	1e-11	–	–	10 second averaging time[3]
Frequency Stability – Stratum 3 Grade						
Frequency Stability over Temperature	F_stab	–	–	±0.2	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range.
		–	–	±0.25	ppm	
Initial Tolerance	F_init	–	–	±1	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±2.5	–	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±0.4	–	ppb	Regulated LVCMOS output, 8 pF ±10%. Clipped sinewave output, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	dF/dT	–	±6.4	±10	ppb/°C	1°C/min temperature ramp rate
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.11	–	ppb/s	1°C/min temperature ramp rate
24-hour holdover stability	F_24_Hold	–	–	±0.28	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±0.8 pF load variation and 24-hour aging
One-Day Aging	F_1d	–	±3	–	ppb	At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±1	–	ppm	At 50°C, after 2-days of continued operation. Aging is measured with respect to day 3
10-Year Aging	F_10y	–	±1.5	–	ppm	
20-Year Aging	F_20y	–	±2	–	ppm	
20-Year Total Stability	F_tot_20y	–	–	±4.6	ppm	Complies with Stratum 3 per GR-1244-CORE. Actual performance is better

Table 1. Output Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Regulated LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.5	1.2	2	ns	20% to 80% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = +3 mA
Output Voltage Low	VOL	–	–	4%	Vdd	IOL = -3 mA
Output Impedance	Z_out_c	–	20	–	Ohms	Impedance looking into output buffer, Vdd = 3.3 V
		–	20	–	Ohms	Impedance looking into output buffer, Vdd = 2.5 V
		–	20	–	Ohms	Impedance looking into output buffer, Vdd = 1.8 V
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	15%	–	25%	1/F_nom	20% to 80% Vdd
Start-up Characteristics						
Start-up Time	T_start	–	5	–	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs from 0 V to Vdd
Output Enable Time	T_oe	–	600	–	ns	F_nom = 10 MHz
Time to Rated Frequency Stability	T_stability	–	10	–	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs
OE Disable Characteristics						
Time to Disable from OE Pin	T_od	–	600	–	ns	

Note:

3. Measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	1.71	1.8	1.89	V	Contact SiTime for 2.25 V to 3.63 V continuous range
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.70	3.0	3.30	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	Idd	–	80	–	mA	F_nom = 19.2 MHz, No Load, TCXO and DCTCXO modes
OE Disable Current	I_od	–	78	–	mA	OE = GND, output weakly pulled down. TCXO, DCTCXO

Table 3. Input and Interface Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – I²C (DCTCXO) modes						
Pull Range	PR	±400	–	–	ppm	DCTCXO mode
Absolute Pull Range[4]	APR	±399.53	–	–	ppm	±0.1 ppm F_stab, DCTCXO for PR = ±400 ppm
		±399.43	–	–	ppm	±0.2 ppm F_stab, DCTCXO for PR = ±400 ppm
		±399.38	–	–	ppm	±0.25 ppm F_stab, DCTCXO for PR = ±400 ppm
Frequency Pull Clamp Limit[5]	PC_L	±3.125, ±6.25, ±10, ±12.5, ±25, ±50, ±100, ±200, ±400			ppm	DCTCXO mode
I²C Interface Characteristics, DCTCXO mode						
Bus Speed	F_I2C	≤ 1000			kHz	SDA capacitance <20 pF
		≤ 400				SDA capacitance <50pF
		≤ 100				SDA capacitance <165 pF
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	
Input Voltage High	VIH_I2C	70%	–	–	Vdd	
Output Voltage Low	VOL_I2C	–	–	10%	Vdd	
Output Voltage High	VOH_I2C	90%	–	–	Vdd	
Input Leakage current	I_I2C_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 $V_{DD.}$ Includes typical leakage current from 200 kΩ pull resister to VDD.
Input Capacitance	C_I2C_{IN}	–	5	–	pF	
Aggregate Pull-Up Impedance	Z_{PU}	5	–	–	kΩ	
SPI Interface Characteristics, DCTCXO mode						
Bus Speed	F_SPI	≤5000			kHz	MISO capacitance < 15 pF
		≤1000			kHz	MISO capacitance < 50 pF
Input Voltage Low	VIL_SPI	–	–	10%	Vdd	
Input Voltage High	VIH_SPI	90%	–	–	Vdd	
Output Voltage Low	VOL_SPI	–	–	10%	Vdd	IOL = 2.7 mA (Vdd = 2.5V)
Output Voltage High	VOH_SPI	90%	–	–	Vdd	IOH = 2.2 mA (Vdd = 2.5V)
Input Capacitance	C_SPI_{IN}		5		pF	
Leakage in High Impedance Mode	I_SPI_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 $V_{DD.}$

Notes:

4. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.
5. Clamp limit is specified at time of order, which prevents pulling the frequency beyond the specified value.

Table 4. Jitter & Phase Noise – Regulated LVCMOS

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	100	–	fs	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
RMS Period Jitter	T_jitt_per	–	1	–	ps	F_nom = 19.2 MHz, measured per JESD65B
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	–	ps	F_nom = 19.2 MHz, measured per JESD65B
Phase Noise						
1 Hz offset		–	-84	–	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-135	–	dBc/Hz	
1 kHz offset		–	-145	–	dBc/Hz	
10 kHz offset		–	-159	–	dBc/Hz	
100 kHz offset		–	-170	–	dBc/Hz	
1 MHz offset		–	-171	–	dBc/Hz	
5 MHz offset		–	-172	–	dBc/Hz	
Spurious	T_spur	–	-105	–	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets, 8 pF ±10%
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[6]	PSJS	–	0.2	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	19.2 MHz, 50 mV peak-peak ripple on VDD

Note:

6. Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 5. Jitter & Phase Noise – Clipped Sinewave

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	100	–	fs	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
Phase Noise						
1 Hz offset		–	-84	–	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-135	–	dBc/Hz	
1 kHz offset		–	-145	–	dBc/Hz	
10 kHz offset		–	-159	–	dBc/Hz	
100 kHz offset		–	-167	–	dBc/Hz	
1 MHz offset		–	-168	–	dBc/Hz	
5 MHz offset		–	-169	–	dBc/Hz	
Spurious	T_spur	–	-105	–	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets, 10 pF ±10%
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[6]	PSJS	–	0.1	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	19.2 MHz, 50 mV peak-peak ripple on VDD

Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 150	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[7]		130	°C
Input Voltage, Maximum	Any input pin	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	V

Note:
7. Exceeding this temperature for an extended period of time may damage the device.

Table 7. Thermal Considerations[8]

Package	θ_{JA}[9] (°C/W)	θ_{JC}, Bottom (°C/W)
Ceramic 5.0 mm x 3.5 mm	TBD	TBD

Notes:
8. Measured in still air. Refer to JESD51 for θ_{JA} and θ_{JC} definitions.
9. Devices soldered on a JESD51 2s2p compliant board.

Table 8. Maximum Operating Junction Temperature[10]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	**85°C**
85°C	**100°C**
105°C	**120°C**

Note:
10. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Temperature Cycle	JESD22, Method A104	–	–
Solderability	MIL-STD-883F, Method 2003	–	–
Moisture Sensitivity Level	MSL1 @260°C	–	–

Device Configurations and Pin-outs

Table 10. Device Configurations

Configuration	Pin 1	Pin 2	Pin 3	Pin 5	Pin 10	I²C and SPI Programmable Parameters
TCXO	OE / NF	NF	NF	NF	NF	–
DCTCXO	OE / NF	SCLK	A1	A0	SDA	I2C: Frequency Pull Range, Frequency Pull Value, Output Enable control
	OE / NF	SCLK	MOSI	$\overline{CS}$ / NF	MISO	SPI: Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-outs (Top View)

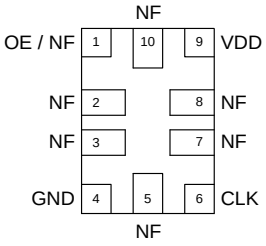


Figure 3. TCXO

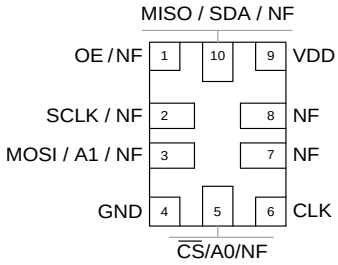


Figure 4. DCTCXO

Table 11. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE / NF[13]	OE – Input	100 kΩ Pull-Up	H[11]: specified frequency output L: output is high impedance. Only output driver is disabled
		NF[13] – No Function	–	H or L or Open: No effect on output frequency or other device functions
2	SCLK / NF[13]	SCLK – Input	200 kΩ Pull-Up	I²C/SPI serial clock input
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions
3	MOSI / A1 / NF[13]	MOSI – Input	100 kΩ Pull-Up	SPI serial data input
		A1 – Input	100 kΩ Pull-Up	I²C address, most significant bit (MSB), when address is selected via pins.
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	–	Connect to ground[14]
5	$\overline{CS}$ / A0 / NF[13]	$\overline{CS}$ – SPI Chip Select	100 kΩ Pull-Up	SPI Chip select, active low
		A0 – Input	100 kΩ Pull-Up	I²C address, least significant bit (LSB), when address is selected via pins. This pin is NF when I²C device address is specified in the ordering code. $\overline{CS}$ is SPI chip select, active low
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions.
6	CLK	Output	–	Regulated LVCMOS, or clipped sinewave oscillator output
7	NF[13]	NF – No Function	–	H or L or Open: No effect on output frequency or other device functions.
8	NF[13]	NF – No Function	–	H or L or Open: No effect on output frequency or other device functions.
9	VDD	Power	–	Connect to power supply[12]
10	MISO / SDA / NF[13]	MISO – Output	–	SPI serial data output
		SDA – Input/Output	200 kΩ Pull Up	I²C Serial Data
		NF – No Function	–	H or L or Open: No effect on output frequency or other device functions

Notes:

11. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NF option.
12. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
13. All NF pins can be left floating and do not need to be soldered down.
14. Vias from the GND pins to the GND plane should be maximized.

Test Circuit Diagrams for Regulated LVCMOS and Clipped Sinewave Outputs

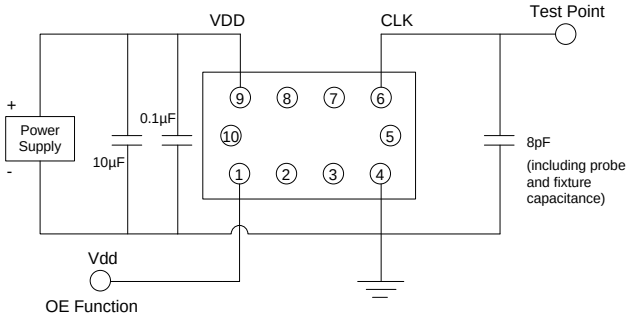


Figure 5. LVCMOS Test Circuit (OE Function)

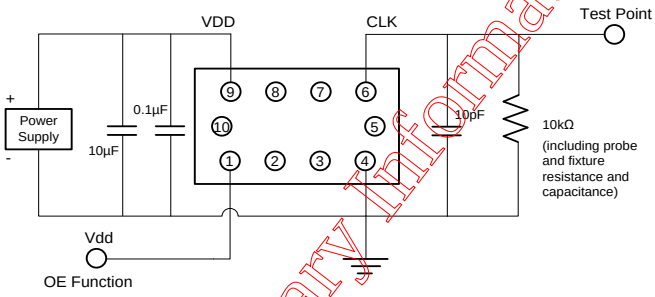


Figure 6. Clipped Sinewave Test Circuit (OE Function) for AC and DC Measurements

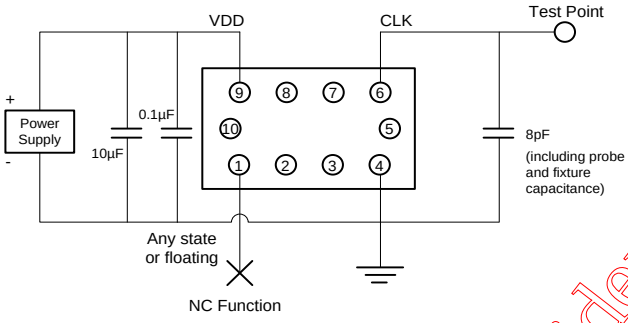


Figure 7. LVCMOS Test Circuit (NF Function)

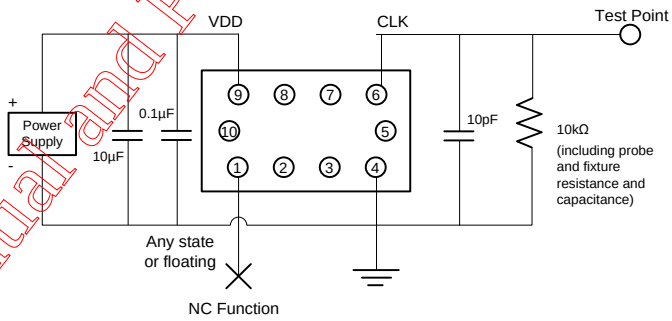


Figure 8. Clipped Sinewave Test Circuit (NF Function) for AC and DC Measurements

Test Circuit Diagrams for Regulated LVCMOS and Clipped Sinewave Outputs (continued)

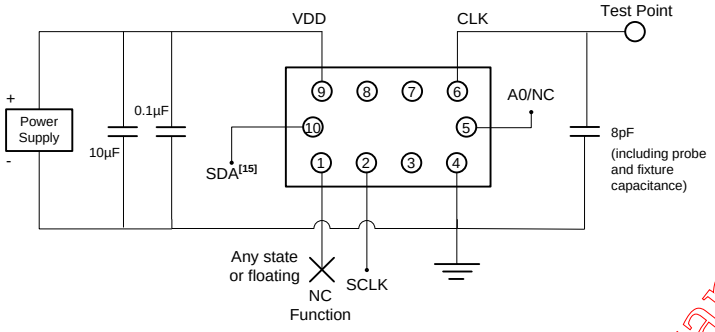


Figure 9. LVCMOS Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

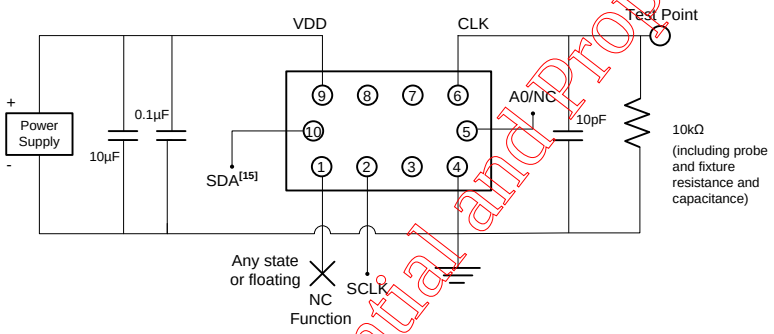


Figure 10. Clipped Sinewave Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

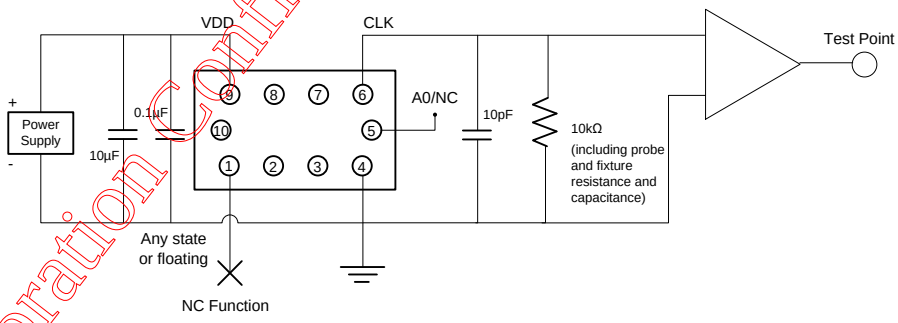


Figure 11. Clipped Sinewave Test Circuit for Phase Noise Measurements, Applies to All Configurations (NF Function shown for example only)

Note:

15. SDA is open-drain and may require pull-up resistor if not present in I²C test setup.

Waveforms

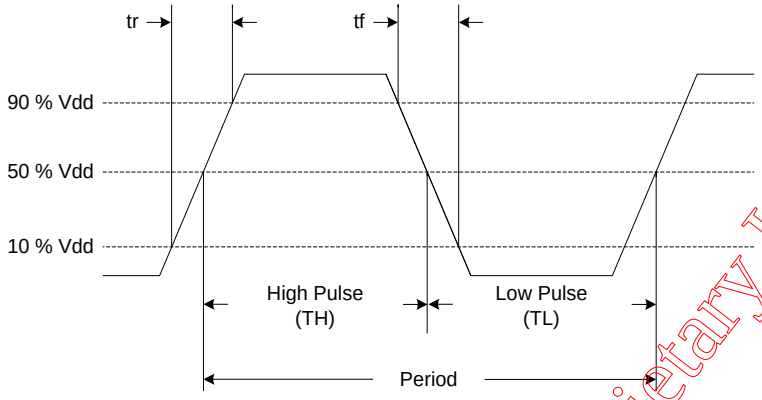


Figure 12. LVCMOS Waveform Diagram[16]

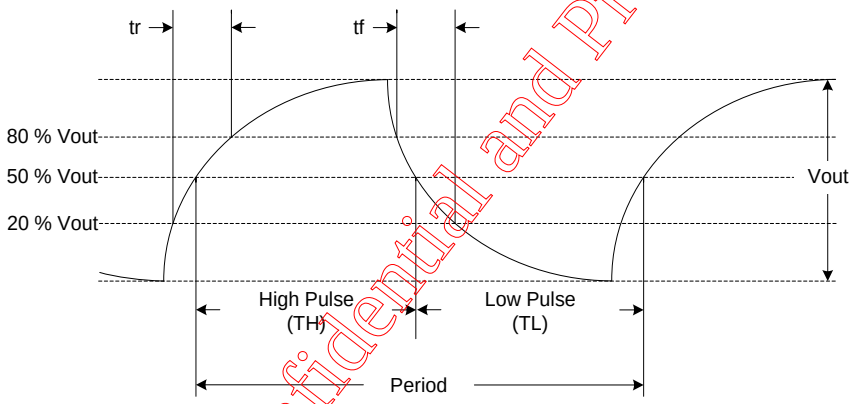
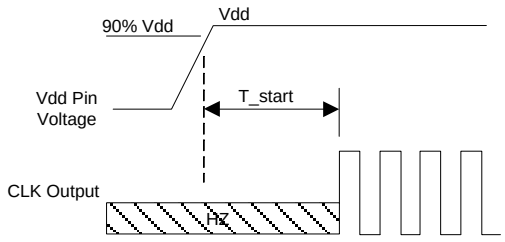


Figure 13. Clipped Sinewave Waveform Diagram[16]

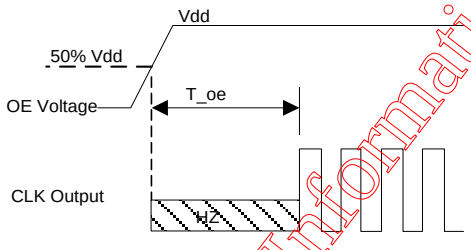
Note:
16. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 14. Startup Timing



T_oe: Time to re-enable the clock output

Figure 15. OE Enable Timing (OE Mode Only)

Stability Diagrams

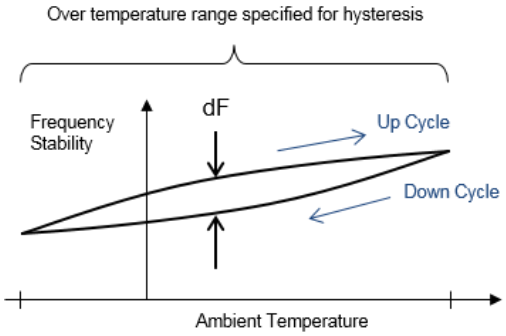
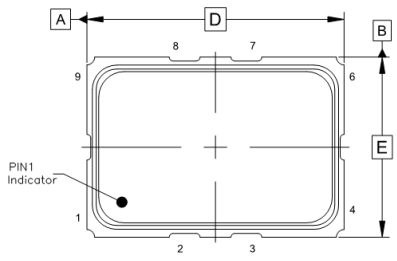


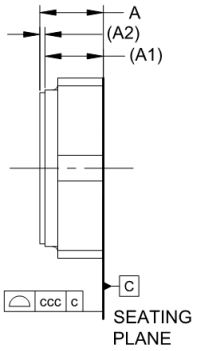
Figure 16. Illustration of hysteresis, where dF is max frequency difference between up and down cycles across temperature

Dimensions and Patterns

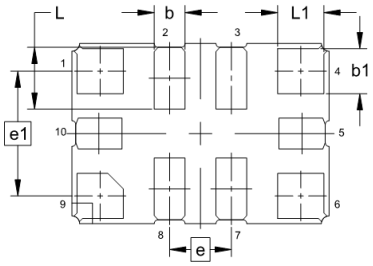
Package Size – Dimensions (Unit: mm)



(TOP VIEW)



(SIDE VIEW)



(BOTTOM VIEW)

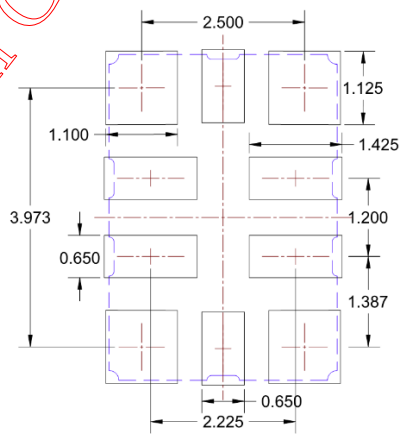
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.095	1.235	1.375
CERAMIC THICKNESS		A1		1.135 ref	
LID THICKNESS		A2		0.100 ref	
BODY SIZE	X	D		5.000 BSC	
	Y	E		3.500 BSC	
LEAD WIDTH		b	0.550	0.600	0.650
		b1	0.825	0.875	0.925
LEAD LENGTH		L	1.150	1.200	1.250
		L1	0.850	0.900	0.950
LEAD PITCH		e		1.200 BSC	
		e1		2.425 BSC	
PACKAGE EDGE TOLERANCE		aaa		0.150	
COPLANARITY		ccc		0.080	

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
10L CQFN 5.000x3.500x1.235 mm		POD-087-CQFN-010-X05035	
		REV	SHEET
DATE	9/8/2021	A01	01

Recommended Land Pattern (Unit: mm)



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
		SPL-087-CQFN-010-C05035	
DATE	10L CQFN 5.000x3.500 mm	REV	SHEET
2023/04/06		A04	01

Additional Information

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 13. Revision History

Version	Release Date	Change Summary
0.1	17-Jun-2020	First release, advanced information
0.11	12-Jul-2020	Revised phase noise
0.12	16-Sep-2020	Revised phase noise
0.13	12-Dec-2020	Revised phase noise
0.14	24-Jun-2021	Updated images in dimensions and patterns
0.15	8-Sep-2021	Updated package image in dimensions and patterns.
0.16	29-Dec-2021	Updated jitter for both LVCMOS and Clipped Sine waveforms Updated current consumption Updated block diagram
0.20	16-Nov-2022	Added "F" packaging option Revised default output load to 8 pF for LVCMOS output Revised F_Vdd and F_load specifications Revised condition for Tr,Tf specification Revised VOL specification Added Note 14
0.21	6-Dec-2022	Revised Sapphire product name to Elite RF™
0.22	20-Apr-2023	Revised LVCMOS output type to “Regulated LVCMOS” from “LVCMOS” Revised VOL spec to a maximum of 4% Added SPI Interface Characteristics Improved land pattern – no dimensions were changed
0.23	6-Jun-23	Updated output frequency range – 10 to 60 MHz Updated F_I2C and Zpu specifications

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439