# SiT9371

Ultra-Low Jitter Differential XO for PCIe Frequencies

## Description

The SiT9371 is a differential oscillator with an integrated MEMS resonator (such as ApexMEMS™), that is engineered for ultra-low-jitter PCIe applications at 100.000000 MHz.

The SiT9371 can be factory programmed for specific combinations of stability, output signaling, voltage, and output enable functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The programmability of this device makes it ideal for communications, enterprise, and industrial applications that require a variety of conditions and operate in noisy environments. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

## Features

- 100.000000MHz standard frequency
- PCIe Gen 1 to 6 compliant
- 15 fs RMS typical phase jitter, per PCIe Gen 5 standard
- 10 fs RMS typical phase jitter, per PCIe Gen 6 standard
- 9 fs/mV typical PSNR
- LVPECL, LVDS, HCSL, Low-power HCSL signaling options.
- ±20, ±25, ±30, and ±50 ppm frequency stabilities
- Wide temperature range (-40°C to 105°C)
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous power supply voltage range options
- 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5 mm x mm package

## Applications

- PCIe Gen 1 to 6
- Compute Express Link (CXL)
- Universal Chiplet Interconnect Express (UCIe)
- Network switches, routers
- Industrial networking equipment
- Server and storage systems
- Test and measurement

Order samples

## Block Diagram

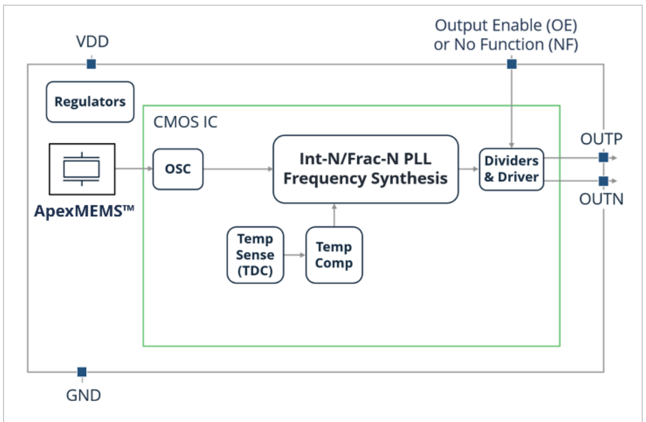



**Figure 1. SiT9371 Block Diagram**

## Package Pinout

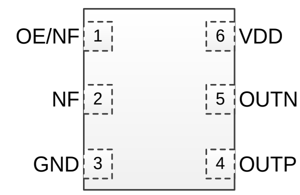



**Figure 2. Pin Assignments (Top view)**
(Refer to Table 13 for Pin Descriptions)

## Ordering Information

**SiT9371AC-01B2-3310-100.000000D**

**Part Family**
"SiT9371"

**Revision Letter**
"A" is the revision of Silicon

**Temperature Range**
"C": Extended Commercial, -20 to 70°C
"I": Industrial, -40 to 85°C
"B": -40 to 95°C
"E": Extended Industrial, -40 to 105°C

**Signaling Group**
"-": LVPECL, LVDS, HCSL, Low-power HCSL

**Signaling Type**
"01": LVPECL
"02": LVDS
"04": HCSL
"08": Low-power HCSL

**Packaging**
Refer to Table 1 for packing method
Leave blank for bulk (for sampling only)

**Frequency**
Refer to the frequencies in Table 2

**Reserved**
"0-": Default

**Pin 1 Functionality**
"0": NF (no function)
"1": OE active high
"2": OE active low

**Supply Voltage**
"18": 1.8 V ± 5%
"25": 2.5 V ±10%
"33": 3.3 V ±10%
"XX": 2.25 V to 3.63 V
"YY": 1.71 V to 3.63 V

**Frequency Stability**
"1": ±20 ppm
"2": ±25 ppm
"8": ±30 ppm
"3": ±50 ppm

**Package Size**[1]
"P": 2.0 x 1.6 mm x mm
"A": 2.5 x 2.0 mm x mm
"B": 3.2 x 2.5 mm x mm

**Note:**
1. Contact SiTime for other package sizes.
2. Contact SiTime for Spread Spectrum option for EMI reduction.

### Table 1. Ordering Codes for Supported Tape & Reel Packing Method

| Device Size (mm x mm) | 8 mm T&R (3ku) | 8 mm T&R (1ku) | 8 mm T&R (250u) |
|---|---|---|---|
| 2.0 x 1.6 | D | E | G |
| 2.5 x 2.0 | D | E | G |
| 3.2 x 2.5 | D | E | G |

### Table 2. Supported Frequencies

| | |
|---|---|
| 100.000000 MHz | |

## Table Of Contents

## Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See Test Circuit Diagrams for the test setups used with each signaling type.

### Table 3. Electrical Characteristics – Common to All Output Signaling Types

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | f | 100.0000 | | | MHz | |
| **Frequency Stability** | | | | | | |
| **Frequency Stability** | F_stab | – | – | ±20 | ppm | Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 2 pF ± 10%, and 10 years aging at 85°C |
| | | – | – | ±25 | ppm | |
| | | – | – | ±30 | ppm | |
| | | – | – | ±50 | ppm | |
| **10 Year Aging** | F_10y | – | ±0.7 | ±2.3 | ppm | Ambient temperature of 85°C |
| **Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended commercial, ambient temperature |
| | | -40 | – | +85 | °C | Industrial, ambient temperature |
| | | -40 | – | +95 | °C | Ambient temperature |
| | | -40 | – | +105 | °C | Extended industrial, ambient temperature |
| **Supply Voltage** | | | | | | |
| **Supply Voltage** | Vdd | 1.71 | – | 3.63 | V | Voltage-supply order code "YY" |
| | | 2.25 | – | 3.63 | V | Voltage-supply order code "XX" |
| | | 1.71 | 1.80 | 1.89 | V | Voltage-supply order code "18". Contact SiTime for 1.5 V |
| | | 2.25 | 2.50 | 2.75 | V | Voltage-supply order code "25" |
| | | 2.97 | 3.30 | 3.63 | V | Voltage-supply order code "33" |
| **Input Characteristics** | | | | | | |
| **Input Voltage High** | VIH | 70% | – | – | Vdd | Logic High function for Pin 1 |
| **Input Voltage Low** | VIL | – | – | 30% | Vdd | Logic High function for Pin 1 |
| **Input Pull-up/Pull-down Impedance** | Z_in | 112.9 | 120 | 133.4 | kΩ | Pin 1 for OE function |
| **Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 48 | – | 52 | % | See Figure 13 for waveform. |
| **Startup, OE and SE Timing** | | | | | | |
| **Startup Time** | T_start | – | 1.2 | 2 | ms | Measured from the time Vdd reaches its rated minimum value |
| **Output Enable Time 1** | T_oe | – | – | 100+3 clock cycles | ns | For all signaling types except Low-Power HCSL. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 19 for waveform. |
| **Output Enable Time 2** | T_oe | – | – | 500+3 clock cycles | ns | For Low-Power HCSL signaling type. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 19 for waveform. |
| **Output Disable Time** | T_od | – | – | 100+3 clock cycles | ns | Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 20 for waveform. |
| **Jitter[3], measured at f = 100 MHz** | | | | | | |
| **PCIe rms Phase Jitter, Gen 6** | T_phj_g6 | – | 10 | 13 | fs | Compare with PCIe Gen 6 (64 GT/s) limit of 100 fs rms |
| **PCIe rms Phase Jitter, Gen 5** | T_phj_g5 | – | 15 | 20 | fs | Compare with PCIe Gen 5 (32 GT/s) limit of 150 fs rms |
| **PCIe rms Phase Jitter, Gen 3 and Gen 4** | T_phj_g3g4 | – | 40 | 50 | fs | Compare with PCIe Gen 4 (16 GT/s) limit of 500 fs rms and Gen 3 (8 GT/s) limit of 1000 fs rms |
| **PCIe rms Phase Jitter, Gen 2** | T_phj_g2 | – | 140 | 165 | fs | Compare with PCIe Gen 2 (5 GT/s) limit of 3100 fs rms |
| **PCIe pp Phase Jitter, Gen 1** | T_phj_g1 | – | 1500 | 1850 | fs | Compare with PCIe Gen 1 (2.5 GT/s) limit of 86,000 fs pp |

**Note:**

3. Measured according to PCI Express Base Specification Revision 6.0.1 common clock requirements documented in section 8.6.7 with jitter filter functions specified in section 8.6.6.2..

**Table 4. Electrical Characteristics – LVPECL |** Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply voltage of 2.5 V. See Figure 4 and Figure 5 for test setups.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| **Current Consumption, Output Enabled without Termination** | Idd_oe_nt | – | 35.5 | 42.5 | mA | Excluding load termination current |
| **Current Consumption, Output Enabled with Termination 1** | Idd_oe_wt1 | – | 46 | 56 | mA | Including load termination current as shown in Figure 23 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms |
| | | – | 46 | 52 | mA | Including load termination current as shown in Figure 23 for Vdd=2.5 V ±10% and R3=220 Ohms |
| **Current Consumption, Output Enabled with Termination 2** | Idd_oe_wt2 | – | 62 | 68 | mA | Including load termination current. See Figure 24 for termination |
| **Current Consumption Output Disabled with Termination 1** | Idd_od_wt1 | – | 53.5 | 65 | mA | Including load termination current as shown in Figure 23 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels. |
| | | – | 53.5 | 61 | mA | Including load termination current as shown in Figure 23 for Vdd=2.5 V ±10% and R3=220 Ohms. Driver output is at logic-high voltage levels. |
| **Current Consumption, Output Disabled with Termination 2** | Idd_od_wt2 | – | 73.5 | 80 | mA | Including load termination current. See Figure 24 for termination. Driver output is at logic-high voltage levels. |
| **Output Characteristics** | | | | | | |
| **Output High Voltage** | VOH | Vdd-1.075 | Vdd-0.95 | Vdd-0.86 | V | See Figure 12 for waveform |
| **Output Low Voltage** | VOL | Vdd-1.84 | Vdd-1.7 | Vdd-1.62 | V | See Figure 12 for waveform |
| **Output Differential Voltage Swing** | V_Swing | 1.4 | 1.5 | 1.65 | V | See Figure 13 for waveform |
| **Rise/Fall Time** | Tr, Tf | – | 170 | 200 | ps | 20% to 80%. See Figure 13 for waveform |
| **Differential Asymmetry, peak-peak** | V_da | – | 45 | – | mV | See Figure 15 for waveform |
| **Differential Skew, peak** | V_ds | – | ±30 | – | ps | See Figure 16 for waveform |
| **Overshoot Voltage, peak** | V_ov | – | 12 | – | % | Measured as percent of V_Swing. See Figure 17 for waveform |
| **Power Supply Noise Immunity** | | | | | | |
| **Power Supply-Induced Jitter Sensitivity** | PSJS | – | 9 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz |
| | | – | 2 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 4 |
| **Power Supply-Induced Phase Noise** | PSPN | – | -79 | – | dBc | 50 mV peak-peak ripple on VDD |
| | | – | -92 | – | dBc | 50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 4 |

**Table 5. Electrical Characteristics – LVDS |** Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal supply of 2.5. See Figure 6 and Figure 7 for test setups.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| **Current Consumption, Output Enabled without Termination** | Idd_oe_nt | – | 32.5 | 39 | mA | Excluding load termination current |
| **Current Consumption, Output Enabled with Termination** | Idd_oe_wt | – | 36 | 42 | mA | Including load termination current. See Figure 26 for termination |
| **Current Consumption Output Disabled with Termination** | Idd_od_wt | – | 42 | 48 | mA | Including load termination current. See Figure 26 for termination. Driver output is at logic-high voltage levels. |
| **Output Characteristics** | | | | | | |
| **Differential Output Voltage** | VOD | 250 | 360 | 450 | mV | See Figure 14 for waveform |
| **Delta VOD** | ΔVOD | – | – | 50 | mV | See Figure 14 for waveform |
| **Offset Voltage** | VOS | 1.125 | 1.25 | 1.375 | V | See Figure 14 for waveform |
| **Delta VOS** | ΔVOS | – | – | 50 | mV | See Figure 14 for waveform |
| **Rise/Fall Time** | Tr, Tf | – | 290 | 330 | ps | Measured 20% to 80% using Figure 26 for termination. See Figure 13 for waveform |
| **Differential Asymmetry, peak-peak** | V_da | – | 25 | – | mV | See Figure 15 for waveform |
| **Differential Skew, peak** | V_ds | – | ±40 | – | ps | See Figure 16 for waveform |
| **Overshoot Voltage, peak** | V_ov | – | 8 | – | % | Measured as percent of VOD. See Figure 18 for waveform |
| **Power Supply Noise Immunity** | | | | | | |
| **Power Supply-Induced Jitter Sensitivity** | PSJS | – | 15 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz |
| | | – | 3.5 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 6 |
| **Power Supply-Induced Phase Noise** | PSPN | – | -75 | – | dBc | 50 mV peak-peak ripple on VDD |
| | | – | -88 | – | dBc | 50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 6 |

**Table 6. Electrical Characteristics – LVDS |** Supply voltage ("order code"): 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal supply of 2.5V. See Figure 6 and Figure 7 for test setups.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| **Current Consumption, Output Enabled without Termination** | Idd_oe_nt | – | 32.5 | 39 | mA | Excluding load termination current |
| **Current Consumption, Output Enabled with Termination** | Idd_oe_wt | – | 36 | 42 | mA | Including load termination current. See Figure 26 for termination |
| **Current Consumption Output Disabled with Termination** | Idd_od_wt | – | 42 | 48 | mA | Including load termination current. See Figure 26 for termination. Driver output is at logic-high voltage levels. |
| **Output Characteristics** | | | | | | |
| **Differential Output Voltage** | VOD | 250 | 330 | 450 | mV | See Figure 14 for waveform |
| **Delta VOD** | ΔVOD | – | – | 50 | mV | See Figure 14 for waveform |
| **Offset Voltage** | VOS | 1.125 | 1.25 | 1.375 | V | See Figure 14 for waveform |
| **Delta VOS** | ΔVOS | – | – | 50 | mV | See Figure 14 for waveform |
| **Rise/Fall Time** | Tr, Tf | – | 290 | 330 | ps | Measured 20% to 80% using Figure 26 for termination. See Figure 13 for waveform |
| **Differential Asymmetry, peak-peak** | V_da | – | 25 | – | mV | See Figure 15 for waveform |
| **Differential Skew, peak** | V_ds | – | ±40 | – | ps | See Figure 16 for waveform |
| **Overshoot Voltage, peak** | V_ov | – | 8 | – | % | Measured as percent of VOD. See Figure 18 for waveform |
| **Power Supply Noise Immunity** | | | | | | |
| **Power Supply-Induced Jitter Sensitivity** | PSJS | – | 17.5 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz |
| | | – | 3.5 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 6 |
| **Power Supply-Induced Phase Noise** | PSPN | – | -73 | – | dBc | 50 mV peak-peak ripple on VDD |
| | | – | -88 | – | dBc | 50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 6 |

**Table 7. Electrical Characteristics – HCSL |** Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"), 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal supply of 2.5V. See Figure 8 and Figure 9 for test setups.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| **Current Consumption, Output Enabled without Termination** | Idd_oe_nt | – | 32 | 38 | mA | Excluding load termination current |
| **Current Consumption, Output Enabled with Termination** | Idd_oe_wt | – | 46.5 | 52 | mA | Including load termination current. See Figure 27 (a) and Figure 27 (b) for termination. |
| **Current Consumption, Output Disabled with Termination** | Idd_od_wt | – | 52.5 | 59 | mA | Including load termination current. See Figure 27 (a) and Figure 27 (b) for termination. Driver output is at logic-high voltage levels. |
| **Output Characteristics** | | | | | | |
| **Output High Voltage** | VOH | 0.60 | 0.7 | 0.95 | V | See Figure 12 for waveform |
| **Output Low Voltage** | VOL | -0.1 | 0 | 0.1 | V | See Figure 12 for waveform |
| **Output Differential Voltage Swing** | V_Swing | 1.1 | 1.4 | 1.6 | V | See Figure 13 for waveform |
| **Rise/Fall Time** | Tr, Tf | – | 340 | 370 | ps | Measured 20% to 80%. See Figure 13 for waveform |
| **Differential Asymmetry, peak-peak** | V_da | – | 65 | – | mV | See Figure 15 for waveform |
| **Differential Skew, peak** | V_ds | – | ±70 | – | ps | See Figure 16 for waveform |
| **Overshoot Voltage, peak** | V_ov | – | 0 | – | % | Measured as percent of V_Swing.<br>See Figure 17 for waveform |
| **Power Supply Noise Immunity** | | | | | | |
| **Power Supply-Induced Jitter Sensitivity** | PSJS | – | 27 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz |
| | | – | 3.5 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 8 |
| **Power Supply-Induced Phase Noise** | PSPN | – | -70 | – | dBc | 50 mV peak-peak ripple on VDD |
| | | – | -88 | – | dBc | 50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 8 |

**Table 8. Electrical Characteristics – Low-Power HCSL |** Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V ±5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V. See Figure 10 and Figure 11 for test setups.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| **Current Consumption, Output Enabled without Termination** | Idd_oe_nt | – | 33 | 38.5 | mA | Excluding load termination current. |
| **Current Consumption, Output Enabled with Termination** | Idd_oe_wt | – | 33.5 | 39 | mA | Including load termination current. See Figure 28 for termination |
| **Current Consumption, Output Disabled with Termination** | Idd_od_wt | – | 35.5 | 42 | mA | Including load termination current. See Figure 28 for termination. Driver output is at logic-high voltage levels. |
| **Output Characteristics** | | | | | | |
| **Output High Voltage** | VOH | 0.8 | 0.9 | 1.15 | V | See Figure 12 for waveform |
| **Output Low Voltage** | VOL | -0.1 | 0 | 0.1 | V | See Figure 12 for waveform |
| **Output Differential Voltage Swing** | V_Swing | 1.6 | 1.83 | 2.0 | V | See Figure 13 for waveform |
| **Rise/Fall Time** | Tr, Tf | – | 330 | 380 | ps | Measured 20% to 80%. See Figure 13 for waveform |
| **Differential Asymmetry, peak-peak** | V_da | – | 55 | – | mV | See Figure 15 for waveform |
| **Differential Skew, peak** | V_ds | – | ±30 | – | ps | See Figure 16 for waveform |
| **Overshoot Voltage, peak** | V_ov | – | 1 | – | % | Measured as percent of V_Swing.<br>See Figure 17 for waveform |
| **Power Supply Noise Immunity** | | | | | | |
| **Power Supply-Induced Jitter Sensitivity** | PSJS | – | 18 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz |
| | | – | 6.5 | – | fs/mV | Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 10 |
| **Power Supply-Induced Phase Noise** | PSPN | – | -73 | – | dBc | 50 mV peak-peak ripple on VDD |
| | | – | -82 | – | dBc | 50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 10 |

## Table 9. Absolute Maximum Ratings

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|
| **Continuous Power Supply Voltage Range (Vdd)** | | -0.5 | 4.0 | V |
| **Input Voltage, Maximum** | Any input pin | – | Vdd + 0.3 | V |
| **Input Voltage, Minimum** | Any input pin | -0.3 | – | V |
| **Storage Temperature** | | -65 | 150 | °C |
| **Maximum Junction Temperature** | | – | 135 | °C |

## Table 10. Thermal Considerations[4]

| Package | $\theta_{JA}$ (°C/W) | $\Psi_{JT}$ (°C/W) | $\theta_{JB}$ (°C/W) | $\theta_{JC,Top}$ (°C/W) |
|---|---|---|---|---|
| **3225, 6-pin** | 101 | 4.7 | 23 | 86 |
| **2520, 6-pin** | 111 | 3.7 | 24 | 116 |
| **2016, 6-pin** | 134 | 3.4 | 24 | 147 |

**Notes:**

4. $\theta_{JA}$, $\Psi_{JT}$, $\theta_{JB}$ and $\theta_{JC}$ are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25C ambient and 250 mW power consumption (typical of 1 GHz $f_{out}$). The conduction thermal resistances $\theta_{JB}$ and $\theta_{JC}$ are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads ($\theta_{JB}$) or the top of the package ($\theta_{JC,Top}$). These may be used in a two-resistor compact model. The values of $\theta_{JA}$ and $\Psi_{JT}$ are strongly application dependent, and we report values based on the JEDEC thermal environment. $\theta_{JA}$ is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. $\Psi_{JT}$ can be used to estimate the junction temperature from measurements of the temperature at the top of the package, if the thermal environment is similar to the JEDEC environment.

## Table 11. Maximum Operating Junction Temperature[5]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|---|---|
| 70°C | 85°C |
| 85°C | 100°C |
| 95°C | 110°C |
| 105°C | 120°C |

**Notes:**

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

## Table 12. Environmental Compliance

| Parameter | Test Conditions | Value | Unit |
|---|---|---|---|
| **Mechanical Shock Resistance** | MIL-STD-883F, Method 2002 | 10,000 | *g* |
| **Mechanical Vibration Resistance** | MIL-STD-883F, Method 2007 | 70 | *g* |
| **Soldering Temperature (follow standard Pb free soldering guidelines)[6]** | MIL-STD-883F, Method 2003 | 260 | °C |
| **Moisture Sensitivity Level** | MSL1 @ 260°C | | |
| **Electrostatic Discharge (HBM)** | HBM, JESD22-A114 | 2,000 | V |
| **Charge-Device Model ESD Protection** | JESD220C101 | 750 | V |
| **Latch-up Tolerance** | JESD78 Compliant | | |

**Notes:**

6. Please refer to SiTime Manufacturing Notes.

## Pin Description

### Table 13. Pin Description

| Pin | Map | Functionality | |
|---|---|---|---|
| 1 | OE/NF | Output Enable (OE) | H[7]: Specified frequency output<br>L[8]: OUT: Logic HIGH, |
| | | No Function (NF) | Open, 120 kΩ internal pull-down resistor to GND |
| 2 | NF | No Function | H or L or Open: No effect on output frequency or other device functions.[9] |
| 3 | GND | Power | Power Supply Ground |
| 4 | OUTP | Output | Oscillator output |
| 5 | OUTN | Output | Complementary oscillator output |
| 6 | VDD | Power | Power supply voltage[10] |

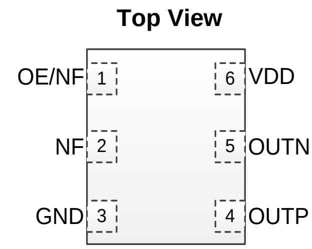



**Figure 3. Pin Assignments**

**Notes:**

7. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, the OE pin is recommended to include an external 10 kΩ resistor (Use 10kΩ pull-up if active high OE; use 10kΩ pull-down if active low OE) when the pin is not externally driven.
8. Differential Logic high means OUTP=VOH, OUTN=VOL.
9. Can be left open. SiTime recommends grounding it for better thermal performance.
10. A capacitor of value 0.1 µF or higher between VDD and GND pins is required.

## Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

### Test Setups for LVPECL Measurements

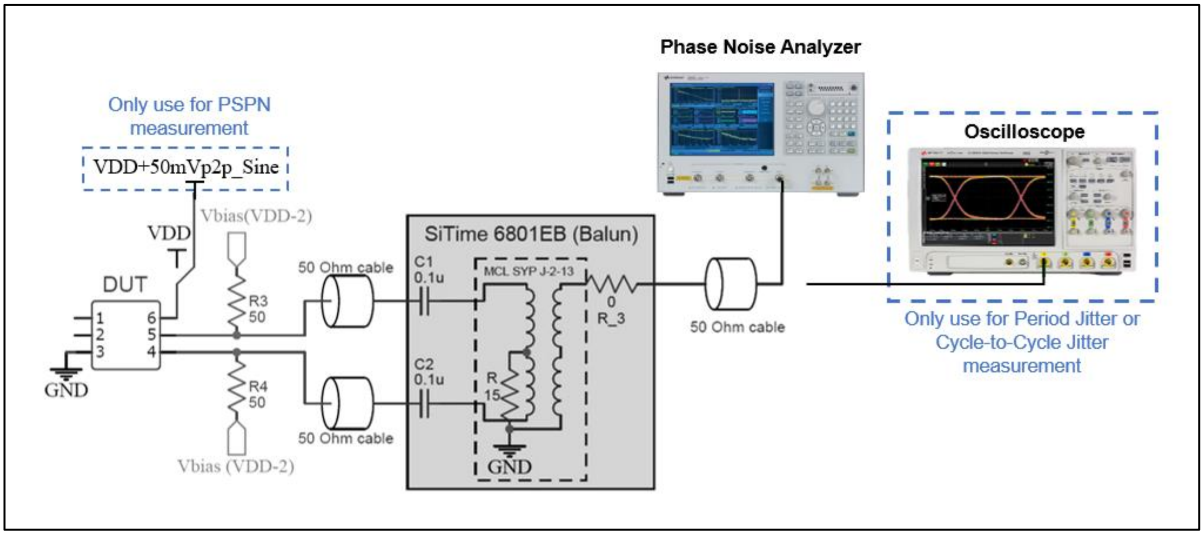



**Figure 4. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) without filter added[11]**

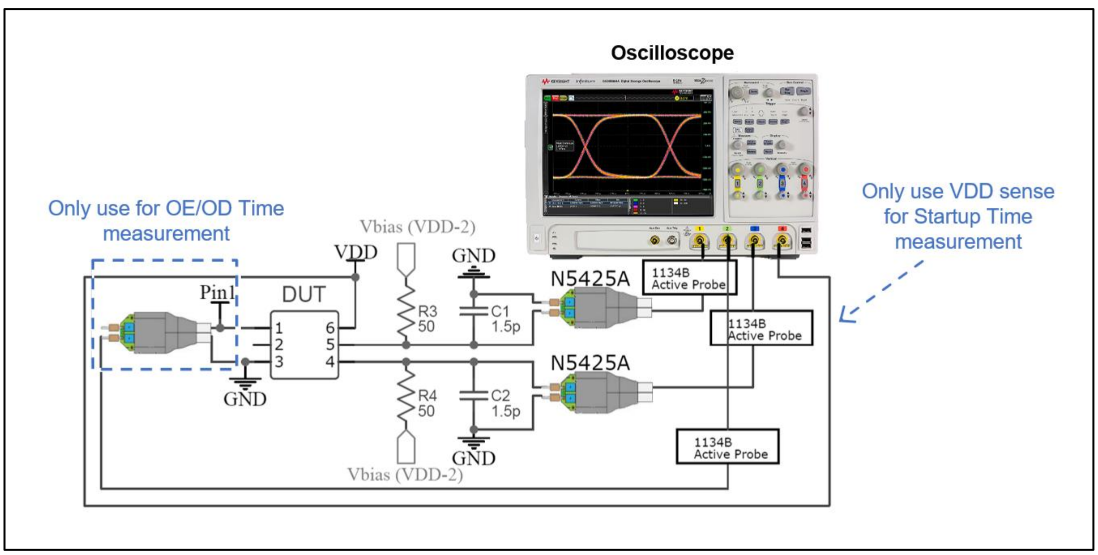



**Figure 5. Test setup to measure LVPECL Waveform Characteristics, Current Consumption (with Termination 2)[12], Output Enable/Disable Time, and Startup Time**

**Notes:**

11. See **Error! Reference source not found.** for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
12. See **Error! Reference source not found.** for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

## Test Circuit Diagrams (continued)

### Test Setups for LVDS Measurements

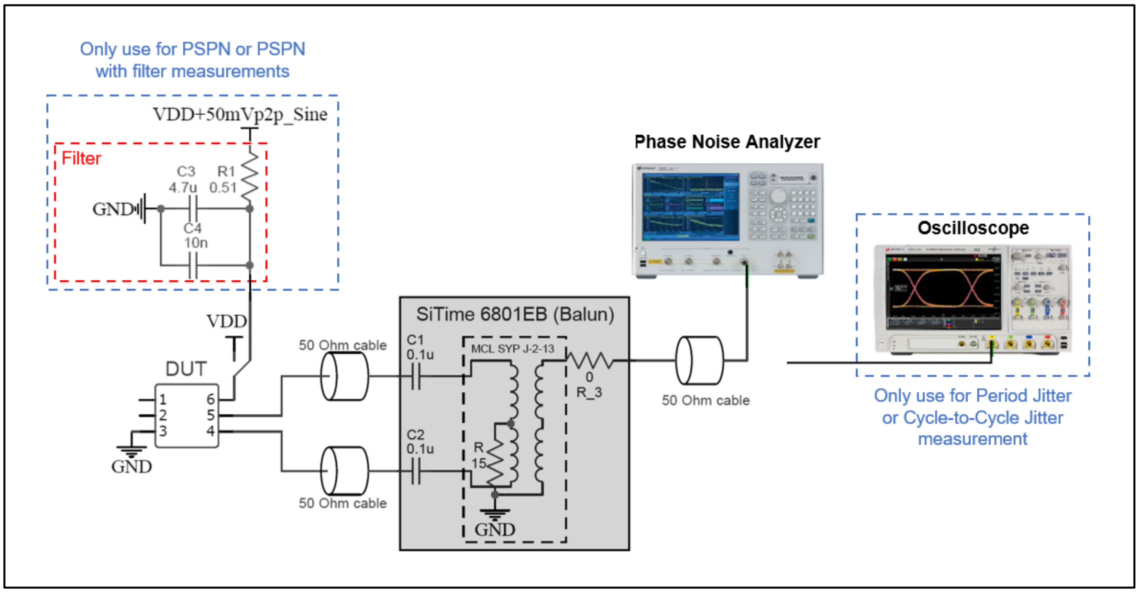



**Figure 6. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added**

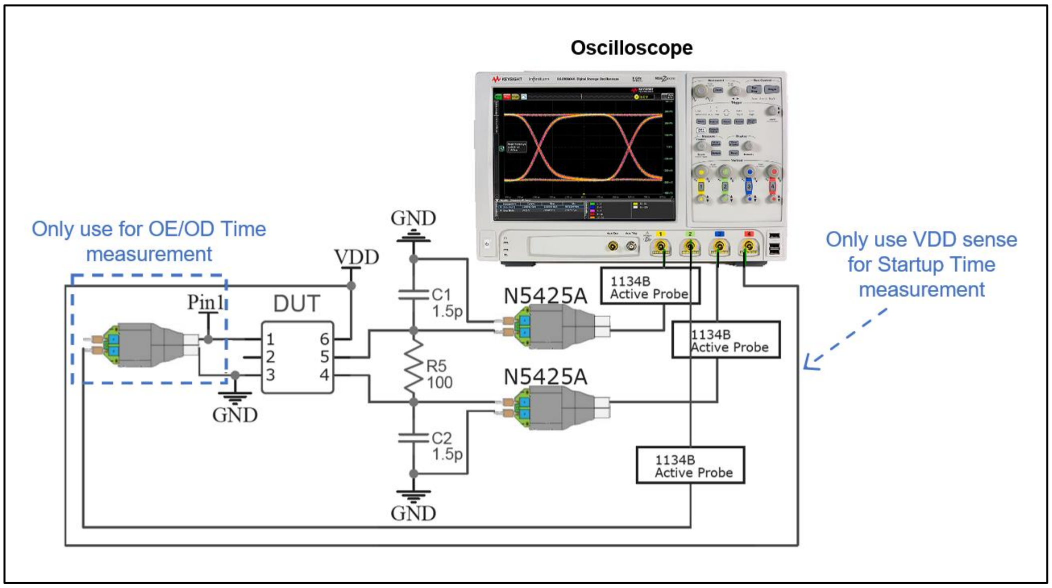



**Figure 7. Test setup to measure LVDS Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time**

## Test Circuit Diagrams (continued)

### Test Setups for HCSL Measurements

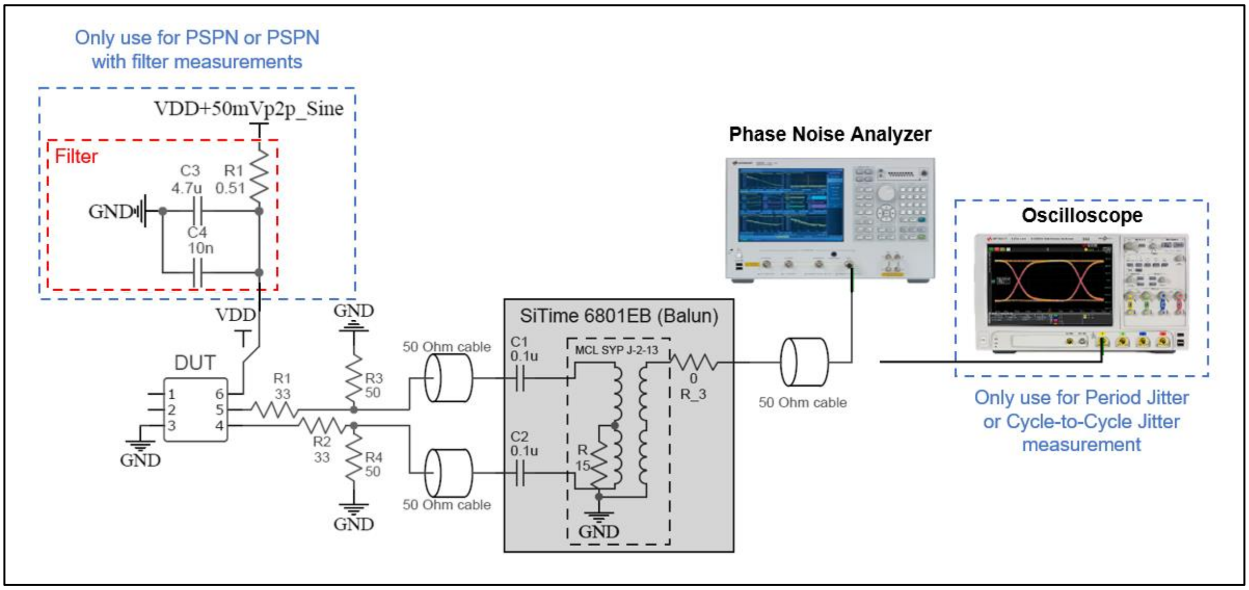



**Figure 8. Test setup to measure HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added**

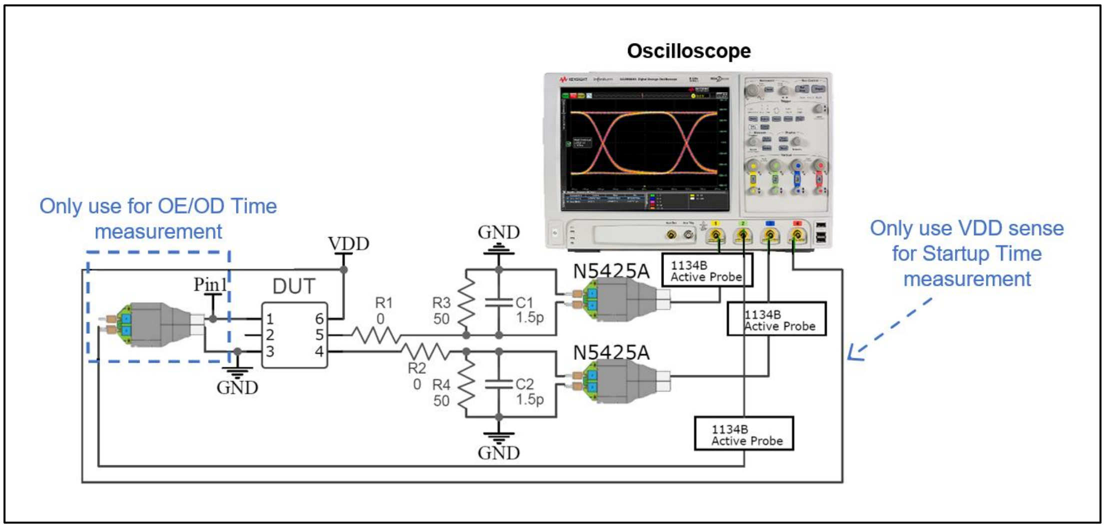



**Figure 9. Test setup to measure HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time**

## Test Circuit Diagrams (continued)

### Test Setups for Low-Power HCSL Measurements

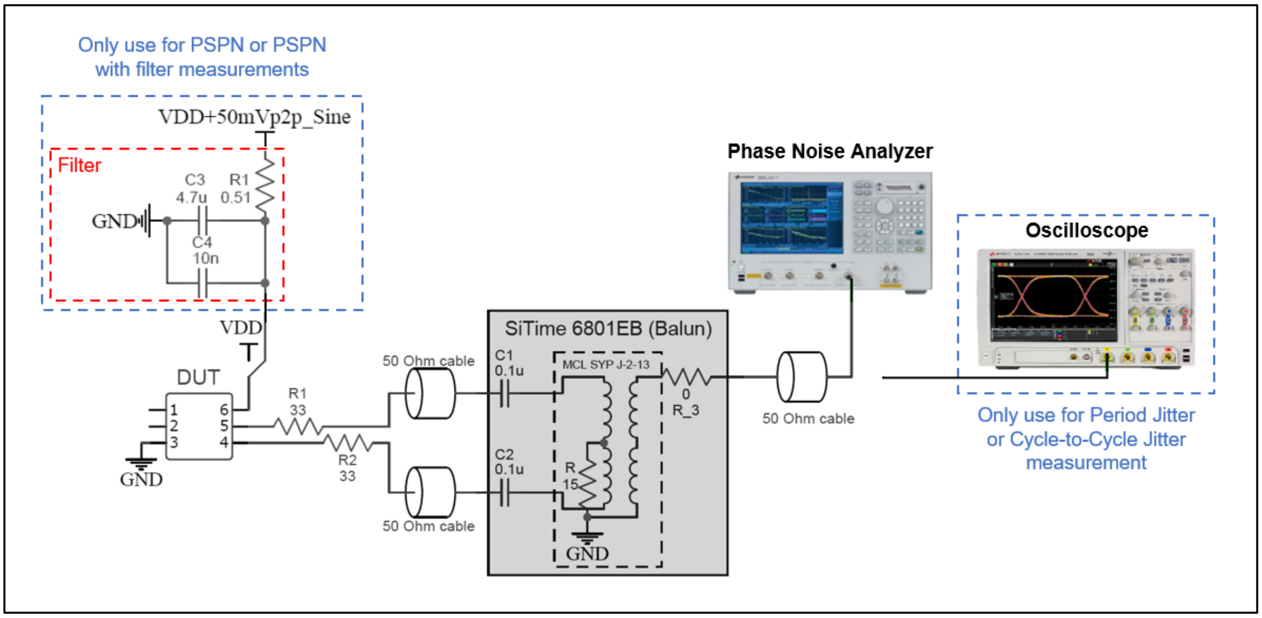



**Figure 10. Test setup to measure Low-Power HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added**

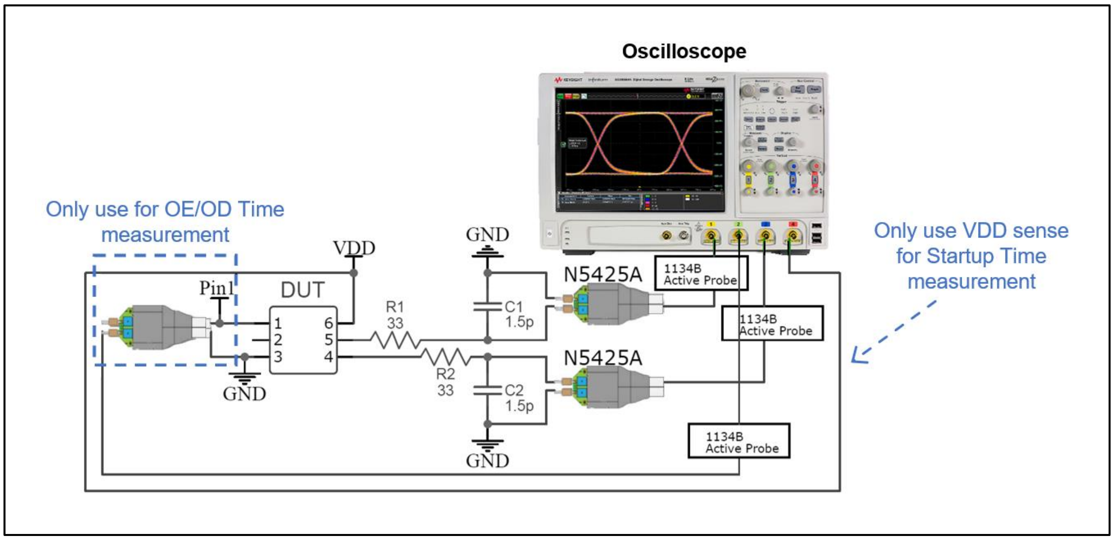



**Figure 11. Test setup to measure Low-Power HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time**

## Waveform Diagrams

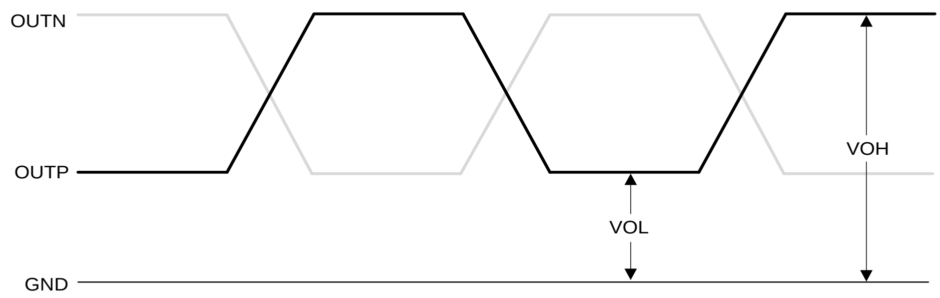



**Figure 12. LVPECL, HCSL, and Low-Power HCSL, Voltage Levels per Differential Pin**

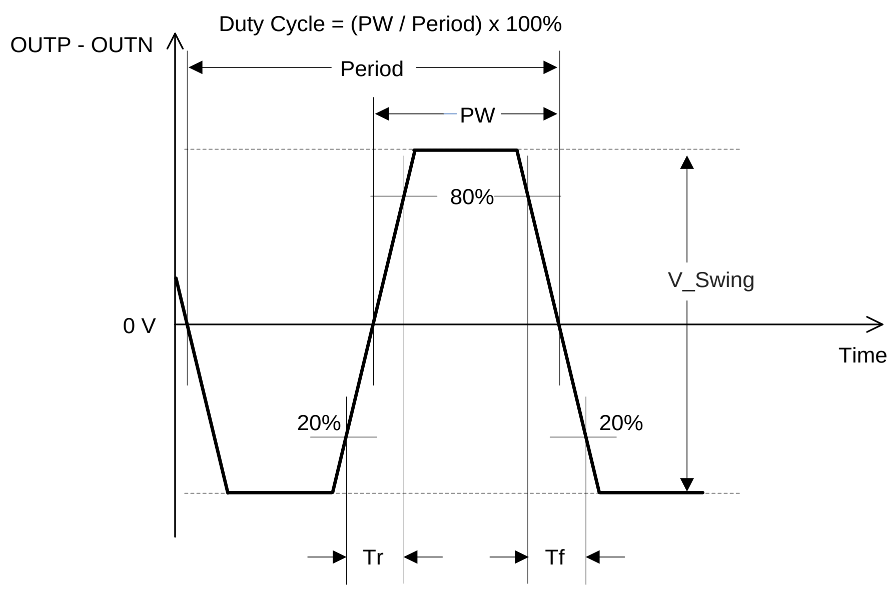



**Figure 13. LVPECL, LVDS, HCSL, and Low-Power HCSL Voltage Levels Across Differential Pair**

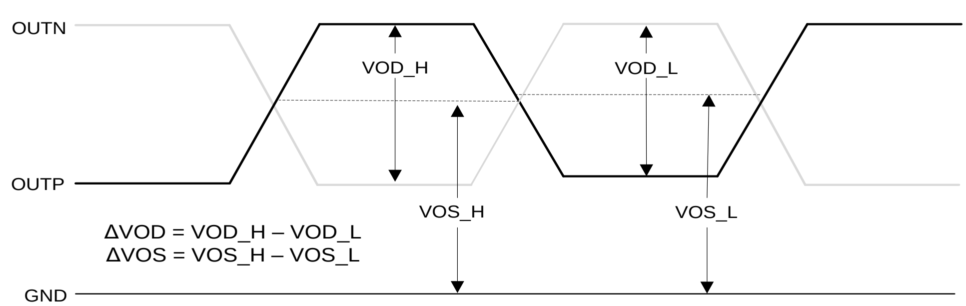



**Figure 14. LVDS Voltage Levels per Differential Pin**

## Waveform Diagrams (continued)

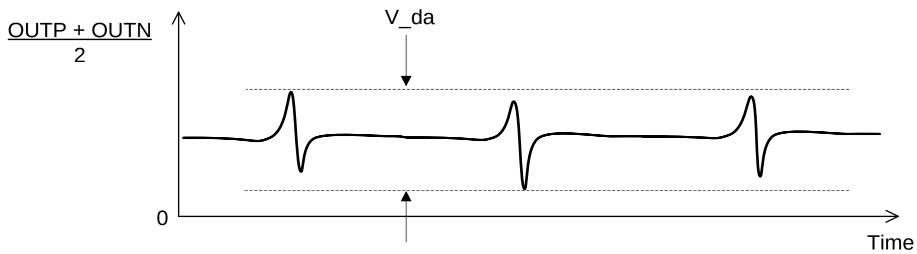



**Figure 15. Differential Asymmetry (V_da)**

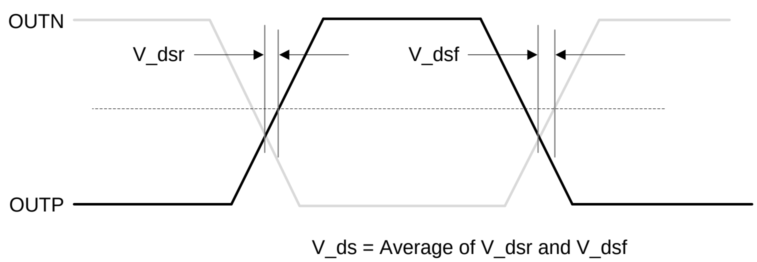



**Figure 16. Differential Skew (V_ds) is measured as the Time between the Average Voltage Level and Crossing Voltage**

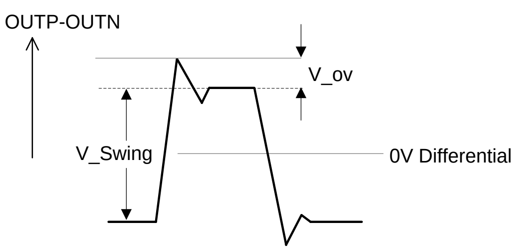



**Figure 17. Overshoot Voltage (V_ov) for LVPECL, , HCSL, Low-power HCSL**

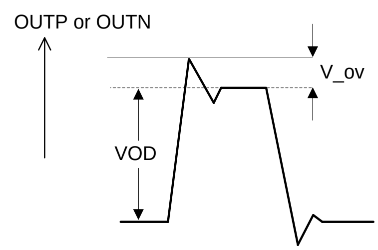



**Figure 18. Overshoot Voltage (V_ov) for LVDS Output**

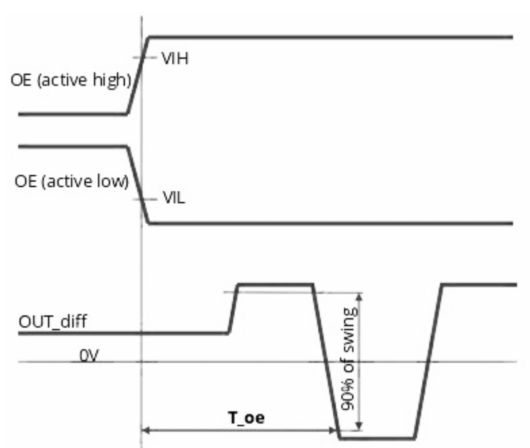



**Figure 19. OE Pin Enable Timing (T_oe)**

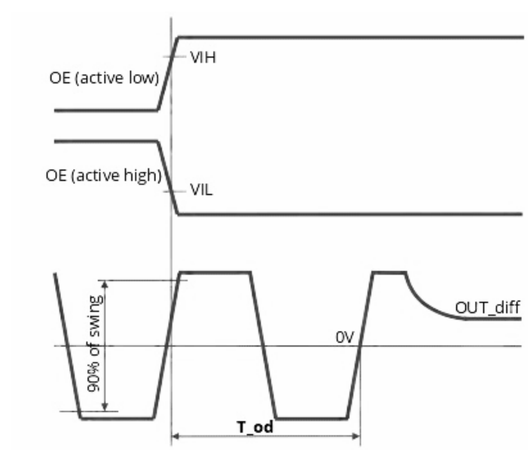



**Figure 20. OE Pin Disable Timing (T_od)**

# Termination Diagrams

## LVPECL Termination

. The table below provides LVPECL current consumption (I_load) into the load termination.

### Table 14. Termination Options for LVPECL Signaling

| Signaling | Supply Voltage Order Codes | Termination Options | | | |
|---|---|---|---|---|---|
| | | Figure 23 | Figure 25 | Figure 26 | Figure 27 |
| **LVPECL referenced to Vdd** | "25", "33", "XX" | OK to use<br>I_load = 40 mA with 100 Ω near-end bias resistor | OK to use<br>I_load = 28mA | OK to use | OK to use<br>I_load = 28mA |

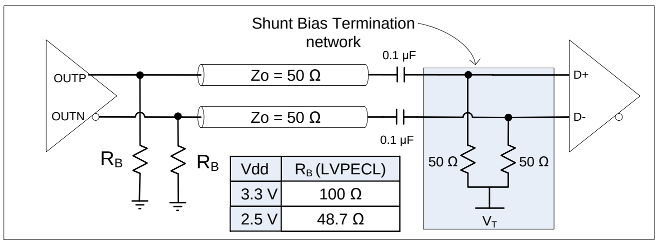



**Figure 21. Recommended LVPECL Termination when AC-coupled**

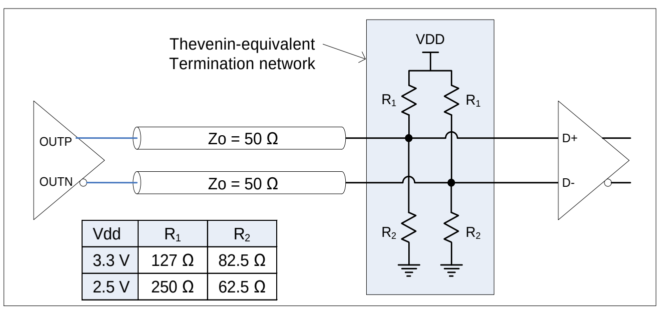



**Figure 22. LVPECL DC-coupled Load Termination with Thevenin Equivalent Network[14]**

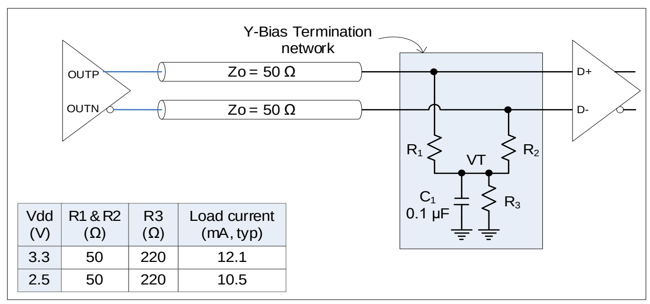



**Figure 23. LVPECL with DC-coupled Parallel Shunt Load Termination**

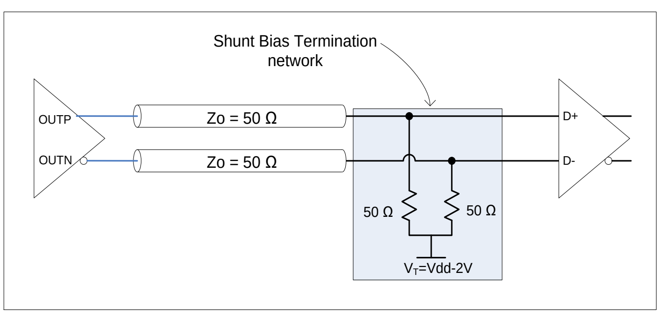



**Figure 24. LVPECL with Y-Bias Termination**

## Termination Diagrams (continued)

### LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

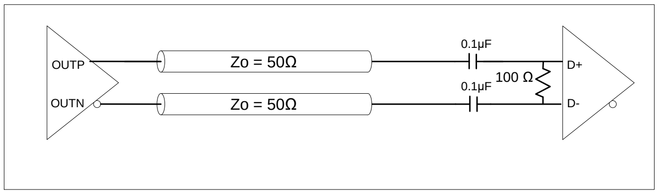



**Figure 25. LVDS AC Termination**

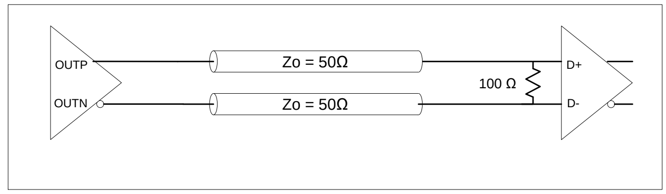



**Figure 26. LVDS DC Termination at the Load**

### HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

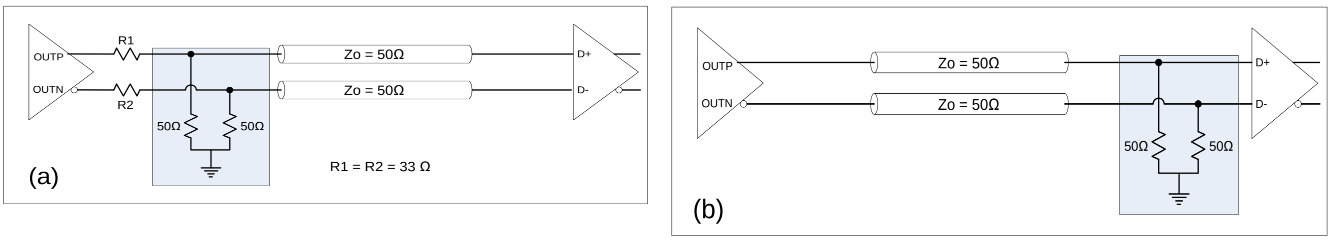



**Figure 27. (a) HCSL Source Termination and (b) HCSL Load Termination**

### Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

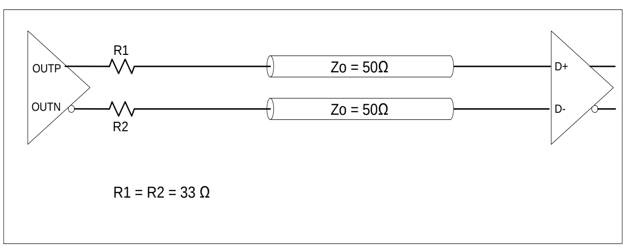


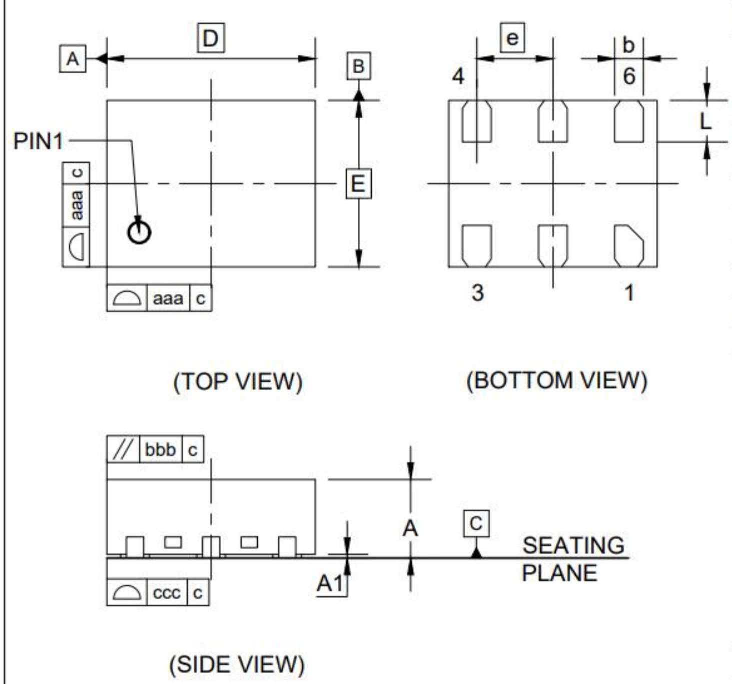

**Figure 28. Low-power HCSL Termination**

**Notes:**

13. Contact SiTime for optimum $R_B$ values for FlexSwing options.
14. Contact SiTime for optimum R1 and R2 values for FlexSwing options.

## Dimensions and Patterns — 2.0 x 1.6 mm x mm

**Package Size – Dimensions (Unit: mm)[15]**



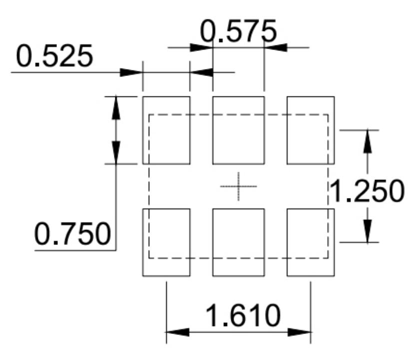

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.700 | 0.750 | 0.800 |
| STAND OFF | | A1 | 0.000 | 0.035 | 0.050 |
| BODY SIZE | X | D | | 2.000 BSC | |
| | Y | E | | 1.600 BSC | |
| LEAD WIDTH | | b | 0.225 | 0.275 | 0.325 |
| LEAD LENGTH | | L | 0.300 | 0.400 | 0.500 |
| LEAD PITCH | | e | | 0.730 BSC | |
| PACKAGE TOLERANCE | | aaa | | 0.100 | |
| MOLD FLATNESS | | bbb | | 0.100 | |
| COPLANARITY | | ccc | | 0.080 | |

NOTE

1. ALL DIMENSION IN MM

| PKG INFO | | DRAWING NO. | |
|---|---|---|---|
| 6L PQFN 2.000x1.600x0.750 mm | | POD-077-PQFN-006-C02016 | |
| | | REV | SHEET |
| DATE | 12/6/2021 | B02 | 01 |

**Recommended Land Pattern (Unit: mm)[16]**




Note : All units in mm.

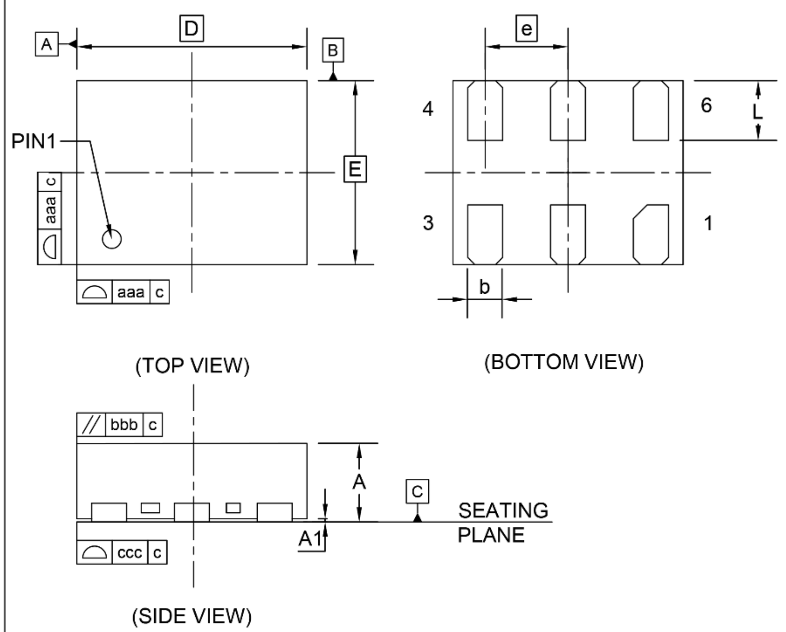
| | PKG INFO | SPL DRAWING NO. | |
|---|---|---|---|
| | 6L QFN 2.000x1.600 mm | SPL-077-QFN-006-C02016 | |
| DATE | | REV | SHEET |
| 2020/04/20 | | B00 | 01 |

**Notes:**

15. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
16. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

## Dimensions and Patterns — 2.5 x 2.0 mm x mm

### Package Size – Dimensions (Unit: mm)[15]




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.800 | 0.850 | 0.900 |
| STAND OFF | | A1 | 0.000 | 0.035 | 0.050 |
| BODY SIZE | X | D | | 2.500 BSC | |
| | Y | E | | 2.000 BSC | |
| LEAD WIDTH | | b | 0.330 | 0.380 | 0.430 |
| LEAD LENGTH | | L | 0.550 | 0.650 | 0.750 |
| LEAD PITCH | | e | | 0.900 BSC | |
| PACKAGE TOLERANCE | | aaa | | 0.100 | |
| MOLD FLATNESS | | bbb | | 0.100 | |
| COPLANARITY | | ccc | | 0.080 | |

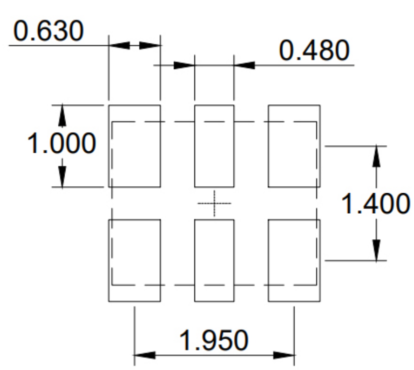
NOTE

1. ALL DIMENSION IN MM

SiTime

| PKG INFO | | DRAWING NO. | |
|---|---|---|---|
| 6L PQFN<br>2.500x2.000x0.850 mm | | POD-092-PQFN-006-C02520 | |
| | | REV | SHEET |
| DATE | 2/28/2024 | A01 | 01 |

### Recommended Land Pattern (Unit: mm)[16]

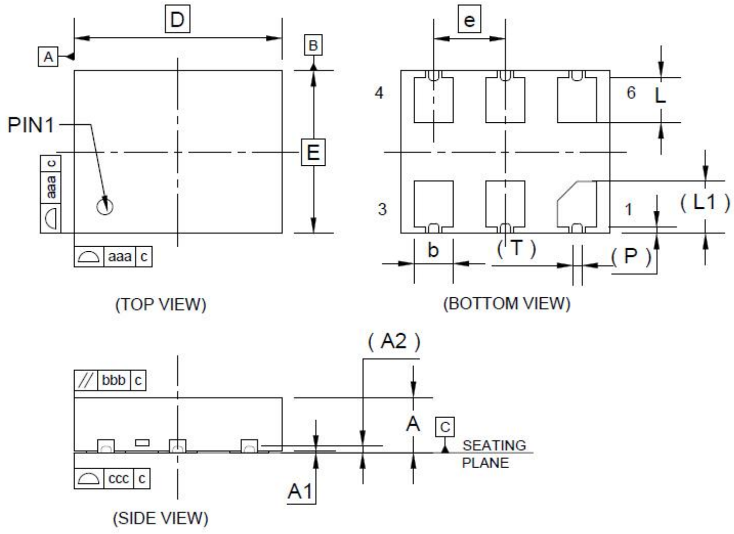



Note : All units in mm.

| SiTime | PKG INFO | SPL DRAWING NO. | |
|---|---|---|---|
| | | SPL-078-QFN-006-C02520 | |
| DATE | 6L PQFW<br>2.500x2.000 mm | REV | SHEET |
| 2021/12/06 | | B00 | 01 |

## Dimensions and Patterns — 3.2 x 2.5 mm x mm

**Package Size – Dimensions (Unit: mm)[15]**



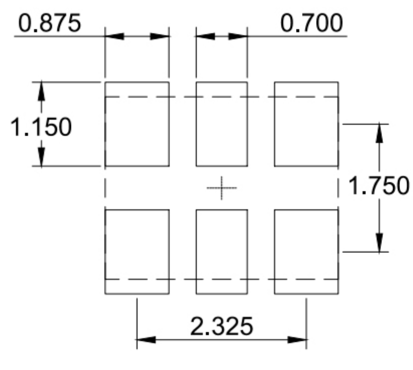

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.800 | 0.850 | 0.900 |
| STAND OFF | | A1 | 0.000 | 0.035 | 0.050 |
| BODY SIZE | X | D | 3.200 BSC | | |
| | Y | E | 2.500 BSC | | |
| LEAD WIDTH | | b | 0.550 | 0.600 | 0.650 |
| LEAD LENGTH | | L | 0.650 | 0.700 | 0.750 |
| | | L1 | 0.800 REF | | |
| LEAD PITCH | | e | 1.100 BSC | | |
| PACKAGE TOLERANCE | | aaa | 0.100 | | |
| MOLD FLATNESS | | bbb | 0.100 | | |
| COPLANARITY | | ccc | 0.080 | | |
| DIMPLE WIDTH | | T | 0.150 REF | | |
| DIMPLE LENGTH | | P | 0.150 REF | | |
| DIMPLE DEPTH | | A2 | 0.100 REF | | |

NOTE
1. ALL DIMENSION IN MM

SiTime

| PKG INFO | | DRAWING NO. | |
|---|---|---|---|
| 6L PQFD 3.200x2.500x0.850 mm | | POD-076-PQFD-006-C03225 | |
| | | REV | SHEET |
| DATE | 10/11/2022 | B01 | 01 |

**Recommended Land Pattern (Unit: mm)[16]**




Note : All units in mm.

| SiTime | PKG INFO | SPL DRAWING NO. | |
|---|---|---|---|
| | | SPL-076-QFN-006-C03225 | |
| DATE | 6L QFN 3.200x2.500 mm | REV | SHEET |
| 2020/04/20 | | B00 | 01 |

## Additional Information

### Table 15. Additional Information

| Document | Description | Download Link |
|---|---|---|
| **ECCN #: EAR99** | Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes. | — |
| **HTS Classification Code: 8542.39.0000** | A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods. | — |
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info | https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products |
| **Termination Techniques** | Termination design recommendations | http://www.sitime.com/support/application-notes |
| **Layout Techniques** | Layout recommendations | http://www.sitime.com/support/application-notes |
| **Evaluation Boards** | SiT6760EB | https://www.sitime.com/support/resource-library/user-manuals/sit6760eb-evaluation-board-user-manual |

## Revision History

### Table 16. Revision History

| Revision | Release Date | Change Summary |
|---|---|---|
| 0.94 | 9-Jan-2023 | Preliminary data sheet |
| 0.95 | 2-Feb-2023 | Updated to include LVPECL and LVDS |
| 0.96 | 17-Apr-2023 | Updated with PCIe standard Gen 1-6; Application to include CXL, UCIe and CK440 |
| 0.97 | 15-May-2023 | Update with PCIe RMS Phase Jitter values for Gen 1 to 6 |
| 1.0 | 28-Feb-2024 | Updated 2520 package Dimensions drawing<br>Updated disclaimer<br>Rev 1.0 Production release |

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