SiT5801

10 to 60 MHz, ± 3 ppb Epoch Platform™ Precision OCXO

ADVANCED

Description

The SiT5801 is the industry's smallest OCXO (9 mm x 7 mm) to offer ±3 ppb over-temp stability, ±0.02 ppb/°C typical frequency slope (dF/dT), and up to 6 hours of time holdover. It is the first OCXO to offer ±3 ppb and ±5 ppb stabilities over a temperature range as wide as -40°C to 95°C. Leveraging SiTime's unique temperature sensing technology and advanced CMOS design, it delivers excellent stability in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The unique modular construction of SiT5801 enables an unmatched combination of class leading stability over temperature, phase noise, programmability, and temperature range all in a compact package. SiT5801 is designed for the best environmental resilience, delivering a precise time reference in the presence of airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT5801's environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible placement on the PCB
- Minimal shielding for thermal isolation

SiT5801 can be factory-programmed to any frequency between 10 MHz and 60 MHz.

Features

- Any frequency between 10 MHz and 60 MHz
- ±3 ppb frequency stability over temperature
- ±0.02 ppb/°C frequency slope typical dF/dT
- Up to 95°C operating temperature range
- Up to 6 hours of holdover over 1.5 µs
- 420 mW power consumption – steady state
- 5E-12 ADEV at 10 second averaging time
- 2.5, 2.8, and 3.3 V supply voltages
- Digital frequency pulling (DCOCXO) via I²C/SPI
  - Up to ±400 ppm pull range
  - Frequency pull resolution down to 0.05 ppt (5e-14)
- Exceptional dynamic stability under airflow and rapid temperature changes
- Integrated regulators for on-chip power-supply noise filtering and excellent PSNR
- Resistant to shock and vibration
- Contact SiTime for ±1 ppb stability option and temperature range up to 105°C

Applications

- 4G/5G access and core networks
- 5G distribution units and 4G base stations
- Network switches and routers
- Hyperscale and edge datacenters
- Passive optical networks
- Time holdover and IEEE 1588 synchronization
- Time and Frequency Measurement

9 mm x 7 mm Package

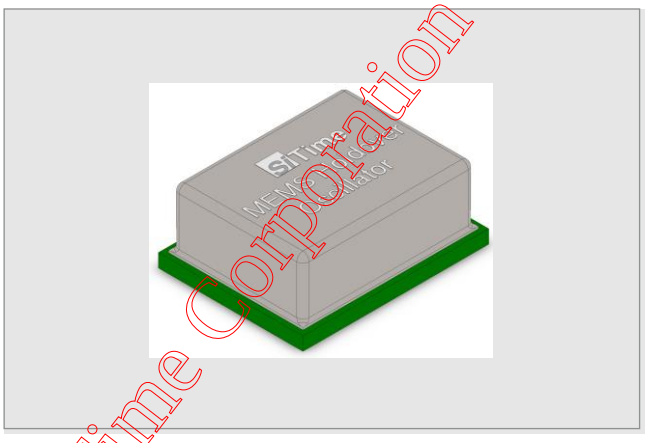


Figure 1. Top and bottom view

Package Pinout

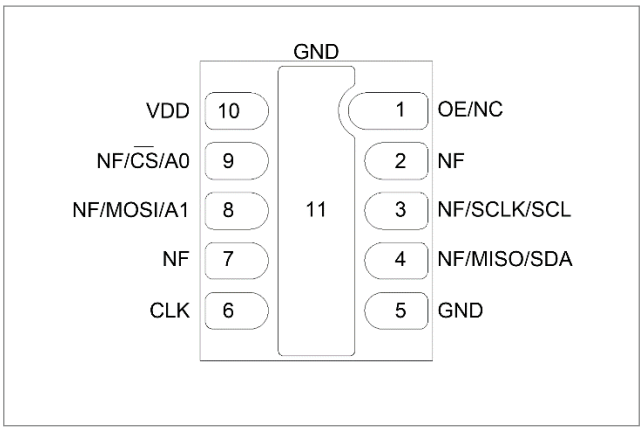
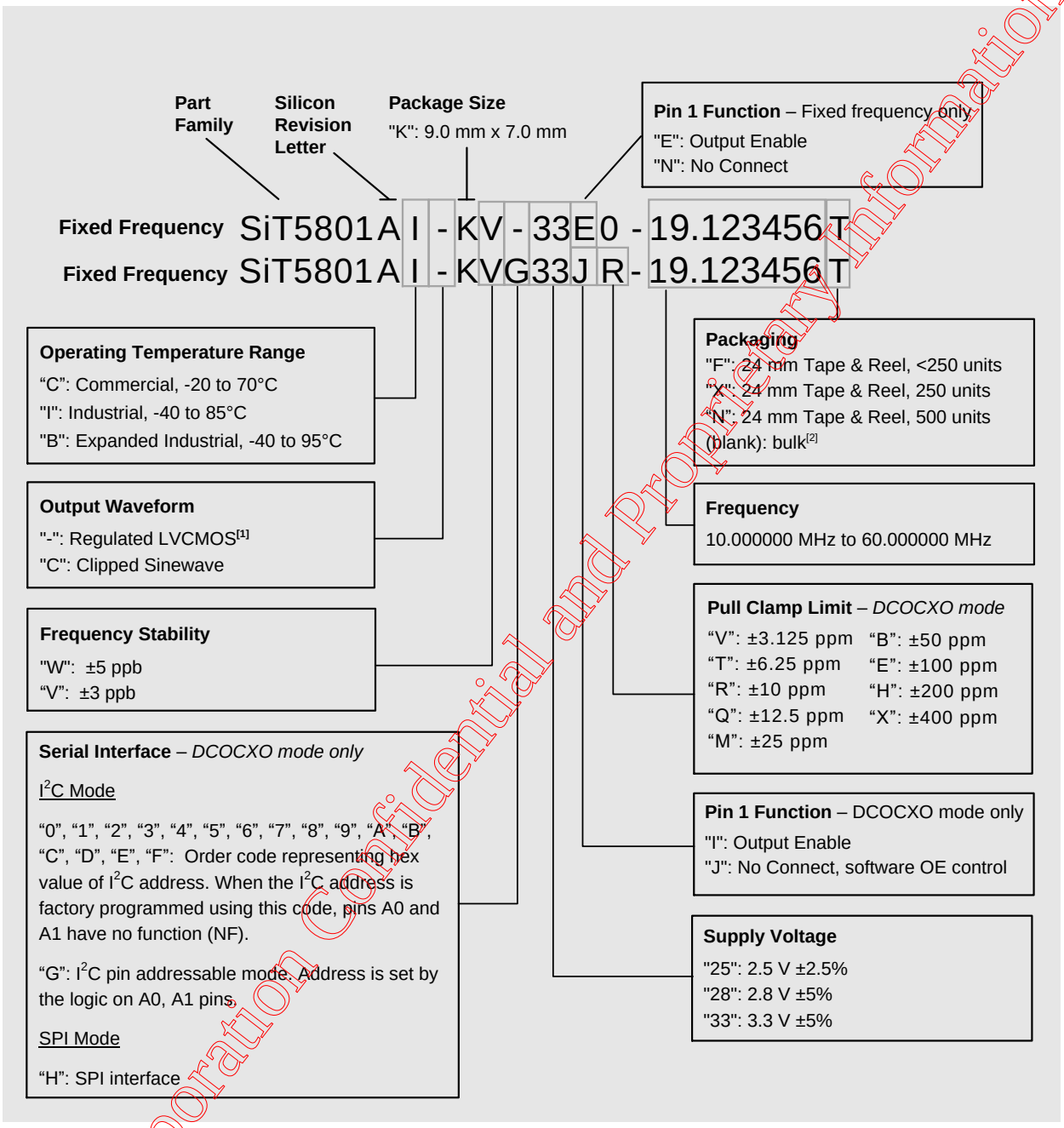


Figure 2. Pin Assignments (Bottom view)

Ordering Information



Notes:

1. "-" corresponds to the default rise/fall time for regulated LVCMOS output as specified in Table 2 (Output Characteristics). Contact SiTime for other rise/fall time options for best EMI.
2. Bulk is available for sampling only.

Table 1. Ordering Codes for Supported Tape & Reel Packaging Method[3]

Device Size	24 mm T&R (<250 units)	24 mm T&R (250 units)	24 mm T&R (500 units)
9 mm x 7 mm	F	X	N

Notes:

3. 10 unit minimum order quantity for tape and reel packaging.

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 8 pF load unless otherwise stated.

Table 2. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	10	–	60	MHz	Contact SiTime for higher frequency options
Temperature Range						
Operating Temperature Range	T_oper	-20		+70	°C	Commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Expanded industrial, ambient temperature
Frequency Stability						
Frequency Stability over Temperature	F_stab	–	–	±3	ppb	Over either operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range.
		–	–	±5		
Initial Tolerance	F_init	–	±0.1	–	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_VDD	–	±0.1	–	ppb	Over operating temperature range (T_oper); VDD ±5%
Output Load Sensitivity	F_load	–	±0.01	–	ppb	Over operating temperature (T_oper); Regulated LVCMOS output, 8 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	–	±0.02	–	ppb/°C	±3 ppb frequency stability over temperature, 0.5°C/min temperature ramp rate, -40 to 95°C
		–	±0.04	–	ppb/°C	±5 ppb frequency stability over temperature, 0.5°C/min temperature ramp rate, -40 to 95°C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.16	–	ppt/s	±3 ppb frequency stability over temperature, 0.5°C/min temperature ramp rate, -40 to 95°C
		–	±0.33	–	ppt/s	±5 ppb frequency stability over temperature, 0.5°C/min temperature ramp rate, -40 to 95°C
Hysteresis Over Temperature Contact SiTime for lower hysteresis	F_hys	–	±0.3	–	ppb	±3 ppb frequency stability over temperature, 0.5°C/min ramp rate, defined as ±ΔF/2
		–	±0.6	–	ppb	±5 ppb frequency stability over temperature, 0.5°C/min ramp rate, defined as ±ΔF/2
One-Day Aging	F_1d	–	±0.4	–	ppb	At 50°C, after 10-days of continued operation. Aging is measured with respect to day 11
		–	±0.3	–	ppb	At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±48	–	ppb	At 50°C, after 2-days of continued operation. Aging is measured with respect to day 3
20-Year Aging	F_20y	–	±80	–	ppb	
Regulated LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	2.4	–	ns	20% - 80% VDD
Output Voltage High	VOH	90	–	–	%	IOH = +3 mA, relative to VDD
Output Voltage Low	VOL	–	–	4	%	IOL = -3 mA, relative to VDD
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	15%	–	25%	1/F_nom	20% - 80% VDD
Start-up Characteristics						
Start-up Time	T_start	–	8	–	ms	Time to first pulse, measured from the time VDD reaches 95% of its final value. VDD ramp time is 100 µs, 0 V to VDD
Time to Frequency Stability	T_stability	–	60	–	s	Time to within rated stability of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement.
		–	100	–	ms	Time to within ±100 ppb of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement.

Table 3. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	VDD	3.14	3.3	3.47	V	Contact SiTime for other voltage options
		2.66	2.8	2.94		
		2.44	2.5	2.56		
Power Consumption						
Power Consumption – Warm Up	Pwr_warmup	–	750	–	mW	F = 20 MHz, 3.3 V, No load, -40°C
Power Consumption – Steady State	Pwr_steady	–	420	–		F = 20 MHz, 3.3 V, No load, 60°C

Table 4. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	2500	kΩ	Internal pull up to VDD
Input High Voltage	VIH	80	–	–	%	
Input Low Voltage	VIL	–	–	20	%	
Frequency Tuning Range – I²C, DCOCXO mode						
Pull Range	PR	±400	–	–	ppm	DCOCXO mode
Absolute Pull Range[4]	APR	±399.82	–	–	ppm	PR = ±400 ppm
Frequency Pull Clamp Limit[5]	PC_L	±3.125, ±6.25, ±10, ±12.5, ±25, ±50, ±100, ±200, ±400			ppm	DCOCXO mode
I2C Interface Characteristics, DCOCXO mode						
Bus Speed	F_I2C	≤ 1000			kHz	SDA capacitance <20 pF
		≤ 400				SDA capacitance <50pF
		≤ 100				SDA capacitance <165 pF
Input Voltage Low	VIL_I2C	–	–	30%	VDD	
Input Voltage High	VIH_I2C	70%	–	–	VDD	
Output Voltage Low	VOL_I2C	–	–	10%	VDD	
Output Voltage High	VOH_I2C	90%	–	–	VDD	
Input Leakage current	I_L	0.5	–	24	µA	0.1 VDD< VOUT < 0.9 VDD. Includes typical leakage current from 200 kΩ pull resister to VDD.
Input Capacitance	C_{IN}	–	5	–	pF	
Aggregate Pull-Up Impedance	Z_{PU}	5	–	–	kΩ	
SPI Interface Characteristics, DCOCXO mode						
Bus Speed	F_SPI	≤ 5000			kHz	MISO capacitance <15 pF
		≤ 1000			kHz	MISO capacitance <50 pF
Input Voltage Low	VIL_SPI	–	–	10%	Vdd	
Input Voltage High	VIH_SPI	90%	–	–	Vdd	
Output Voltage Low	VOL_SPI	–	–	10%	Vdd	IOL = 2.7 mA (Vdd = 2.5V)
Output Voltage High	VOH_SPI	90%	–	–	Vdd	IOH = 2.2 mA (Vdd = 2.5V)
Input Capacitance	C_SPI_{IN}		5		pF	
Leakage in High Impedance Mode	I_SPI_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}.

Notes:

4. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.
5. Clamp limit is specified at the time of order, which prevents pulling the frequency beyond the specified value.

Table 5. Allan Deviation and Phase Noise – Regulated LVCMOS Output

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Allan Deviation						
$\tau = 1$ *second*	AD_1s	–	5E-12	–		
$\tau = 10$ *seconds*	AD_10s	–	5E-12	–		
$\tau = 100$ *seconds*	AD_100s	–	5E-12	–		
Phase Noise						
1 Hz offset		–	-86	–	dBc/Hz	F = 19.2 MHz
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-131	–	dBc/Hz	
1 kHz offset		–	-143	–	dBc/Hz	
10 kHz offset		–	-157	–	dBc/Hz	
100 kHz offset		–	-167	–	dBc/Hz	
1 MHz offset		–	-168	–	dBc/Hz	
5 MHz offset		–	-170	–	dBc/Hz	

Table 6. Allan Deviation and Phase Noise – Clipped Sinewave Output

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Allan Deviation						
$\tau = 1$ *second*	AD_1s	–	5E-12	–		
$\tau = 10$ *seconds*	AD_10s	–	5E-12	–		
$\tau = 100$ *seconds*	AD_100s	–	5E-12	–		
Phase Noise						
1 Hz offset		–	-86	–	dBc/Hz	F = 19.2 MHz
10 Hz offset		–	-113	–	dBc/Hz	
100 Hz offset		–	-131	–	dBc/Hz	
1 kHz offset		–	-143	–	dBc/Hz	
10 kHz offset		–	-157	–	dBc/Hz	
100 kHz offset		–	-167	–	dBc/Hz	
1 MHz offset		–	-167	–	dBc/Hz	
5 MHz offset		–	-168	–	dBc/Hz	

Pin-out Bottom View

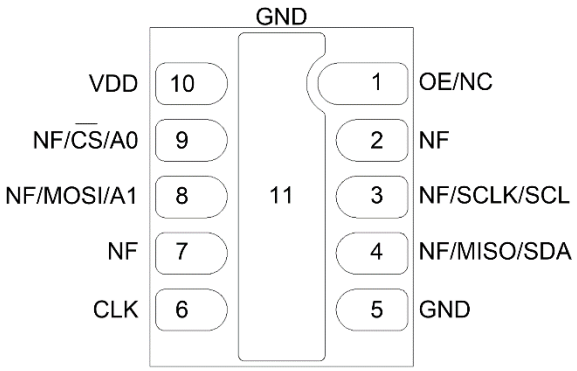


Figure 3. Size 9 mm x 7 mm

Table 7. Pin Assignments

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11
OE/NC	NF	NF/SCLK/SCL	NF/MISO/SDA	GND	CLK	NF	NF/MOSI/A1	NF/$\overline{CS}$/A0	VDD	GND

Table 8. Pin Description

Symbol	I/O	Internal Pull-up Resistor	Function
OE	OE - Input	100 kΩ Pull-Up	H[7]: specified frequency output L: output is high impedance. Only output driver is disabled.
NC	NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions[8]
NF	NF – No Function	-	Solder to pads. Connect to VDD or leave open[6][9]
SCLK	SCLK – Input	200 kΩ Pull-Up	SPI serial clock
SCL	SCL – Input	200 kΩ Pull-Up	I²C serial clock
MISO	MISO – Output	–	SPI serial data
SDA	SDA – Input/Output	200 kΩ Pull Up	I²C Serial data
GND	Ground	-	Connect to ground[10]
CLK	Output	-	Regulated LVCMOS, or clipped sinewave oscillator output
MOSI	MOSI – Input	100 kΩ Pull-Up	SPI serial data input
A1	A1 – Input	100 kΩ Pull-Up	I²C address, most significant bit (MSB), when address is selected via pins
$\overline{CS}$	$\overline{CS}$ – SPI Chip Select	100 kΩ Pull-Up	SPI Chip select, active low
A0	A0 – Input	100 kΩ Pull-Up	I²C address, least significant bit (LSB), when address is selected via pins
VDD	Power	-	Connect to VDD[11]

Notes:

6. If Pin 7 is connected to VDD, a 2 µA leakage current should be expected.
7. In OE mode, a pull-up resistor of 100 kΩ or less is recommended if Pin 1 is not externally driven. If Pin 1 needs to be left floating, use the NC option.
8. Pin 1 voltage should not exceed device VDD or fall lower than device GND. Either of these conditions may lead to frequency shifts larger than specified limits.
9. If connected to VDD, SiTime recommends using narrow traces (e.g. 4 to 6 mil) to avoid significant heat dissipation through these pads.
10. Vias from the GND pins to the GND plane should be maximized.
11. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND.

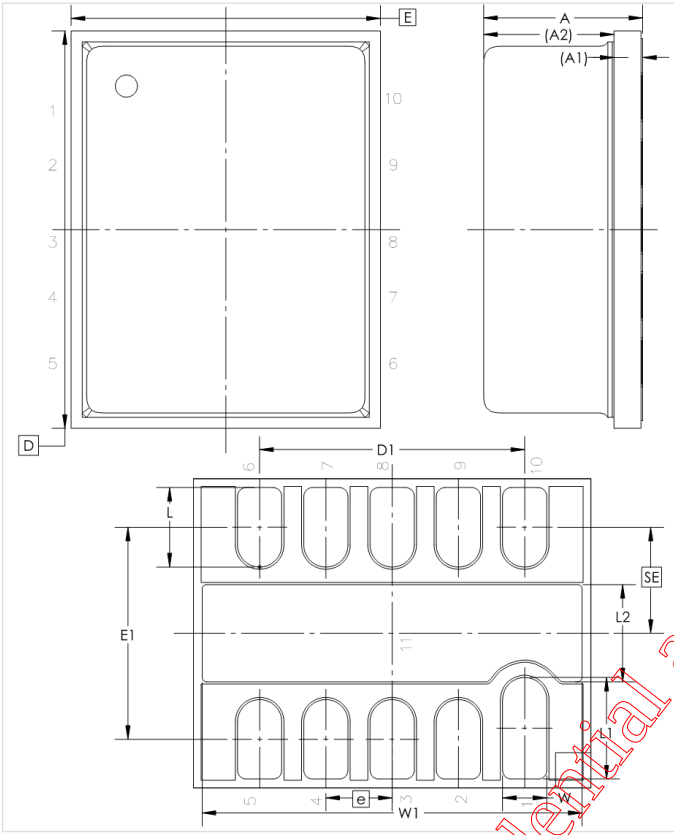
Board Design Guidelines

For optimal device performance, SiTime recommends adhering to the following board design guidelines. These guidelines ensure that heat generated by SiT5801 is sufficiently expelled through the board.

- The metal layer directly below SiT5801 is a ground plane (e.g., If SiT5801 is seated on M1, M2 is a ground plane).
- The ground plane should be continuous in the 9x7 mm area directly under the device.
- Thermal vias are uniformly distributed across the thermal pad. The distance between vias is less than 1.2 mm.
- For a board with more than eight metal layers, at least three are plane layers.
- The metal density in plane layers is maximized.

Dimensions and Patterns — 9 mm x 7 mm package

Package Size – Dimensions (Unit: mm)



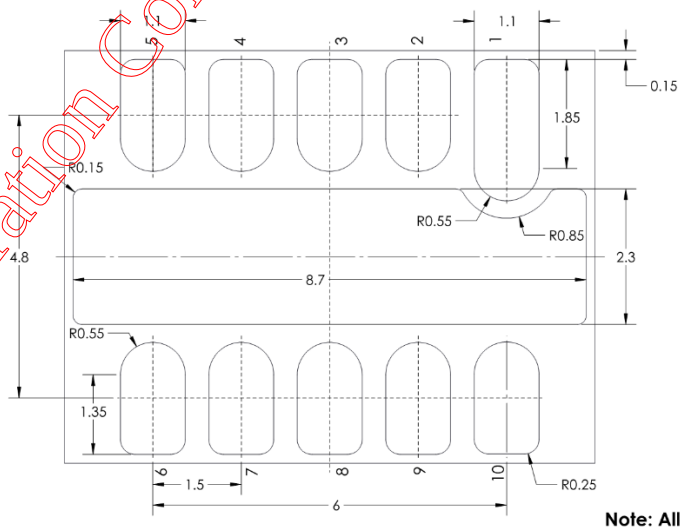
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	3.47	3.6	3.73
SUBSTRATE THICKNESS		A1		0.648 ref.	
LID THICKNESS		A2		2.912 ref	
BODY SIZE	X	D		9 BSC	
	Y	E		7 BSC	
LEAD WIDTH		W	0.950	1.000	1.050
		W1	8.550	8.600	8.650
LEAD LENGTH		L	1.750	1.800	1.850
		L1	2.250	2.300	2.350
		L2	2.150	2.200	2.250
LEAD PITCH		e		1.5 BSC	
EDGE LEAD TO LEAD		D1		6.0 BSC	
		E1		4.8 BSC	
BODY CENTER TO CONTACT LEAD		SE		2.4 BSC	
PACKAGE EDGE TOLERANCE		aaa		0.100	
COPLANARITY		ccc		0.080	

NOTE

1. ALL DIMENSIONS IN MM

SiTime		
PKG INFO		DRAWING NO.
10L PCBA 9.00X7.00X3.60 mm		POD-089-PCBA-010-C09070
		REV / SHEET
DATE	05/03/2023	B01 / 01

Recommended Land Pattern (Top View)



Note: All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.
	10L PCBA 9.0X7.0 mm	SPL-089-PCBA-010-C09070
DATE		REV / SHEET
05/03/2023		B03 / 01

Table 9. Revision History

Version	Release Date	Change Summary
0.1	22-Feb-2022	First release, advanced information
0.11	24-Feb-2022	Resolved typographical error regarding supply voltage and table numbering
0.2	7-Oct-22	Added digital control mode “coming soon” to the ordering information Revised phase noise based on most recent simulations Note 9 added regarding connection of pin 11 to ground Added board design guidelines
0.22	9-Nov-22	Revised ΔF/ΔT specifications Revised Pwr_warmup and Pwr_steady specifications Revised package image Revised package pinout Added ordering information for DCOCXO mode Revised ordering information for packaging Added ΔF/ΔT, F_dynamic, F_hys specifications for ±5 ppb F_stab option Revised condition for Tr and Tf speicifications Revised VOL specifications Revised conditions for T_start and T_stability specifications Revised VDD limits to ±5% Added input characteristics for digital control options Revised phase noise specifications Revised pin assignments and pin descriptions Revised dimensions and patterns
0.23	10-Jan-23	Revised pin out diagram in figures 2 and 3 Revised recommended land pattern
0.24	22-Feb-23	Measured LVCMOS output load revised to 8 pF from 15 pF Revised LVCMOS output type to “Regulated LVCMOS” from “LVCMOS” Revised VOL spec to a maximum of 4% Revised phase noise specifications based on latest measurements Revised 2.5V VDD min/max limits to ±2.5% from ±5% Improved recommended land pattern – no dimensions were changed
0.25	20-Apr-23	Added SPI interface specifications
0.26	5-May-23	Updated package drawing revision – no dimensions were changed Resolved typographical error in the recommended land pattern
0.27	6-June-23	Updated output frequency range – 10 to 60 MHz Updated steady state power consumption Updated F_I2C and Zpu specifications Updated phase noise at 1, 10, and 100 Hz offsets Added table 6 – ADEV and phase noise for clipped sinewave output
0.28	8-Sep-2023	Revised holdover in features section

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