

Description

The SiT5721 is the industry’s first digitally controlled OCXO (DCOCXO), enabling output frequency tuning via I²C interface with ±5 ppt (±0.005 ppb) resolution. The device delivers ±5 ppb over-temp stability, ±0.04 ppb/°C frequency slope (dF/dT) and Stratum 3E compliance in the smallest 9 mm x 7 mm package.

Leveraging SiTime’s unique DualMEMS™ and TurboCompensation™ temperature sensing technology, the SiT5721 is engineered for the best dynamic performance, delivering the most stable timing in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT5721’s environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible placement on the PCB
- Minimal shielding for thermal isolation

SiT5721 can be factory-programmed to any nominal output frequency between 1 MHz and 60 MHz. It is supported by the SiT6731 evaluation board.

Features

- Any frequency between 1 MHz and 60 MHz, in 1 Hz steps
- ±0.04 ppb/°C frequency slope typical (dF/dT)
- ±5 ppb frequency stability over temperature
- Up to 85°C operating temperature range
- 1.5E-11 ADEV at 10 second averaging time
- Digital frequency pulling via I²C
 - ±6.25 ppm pull range
 - ±5 ppt pulling resolution
- Exceptional dynamic stability under airflow and rapid temperature changes
- Excellent Holdover over a wide range of conditions
- Integrated regulators for on-chip power-supply noise filtering and excellent PSRR
- GR-1244 Stratum 3E compliant
- Resistant to shock, vibration and board bending
- 3.3 V supply voltage
- LVCMOS or clipped sinewave output

Applications

- 4G/5G radio
- Base Stations
- Digital Switching
- Time and Frequency Measurement
- IEEE 1588
- Test and measurement

9 mm x 7 mm Package

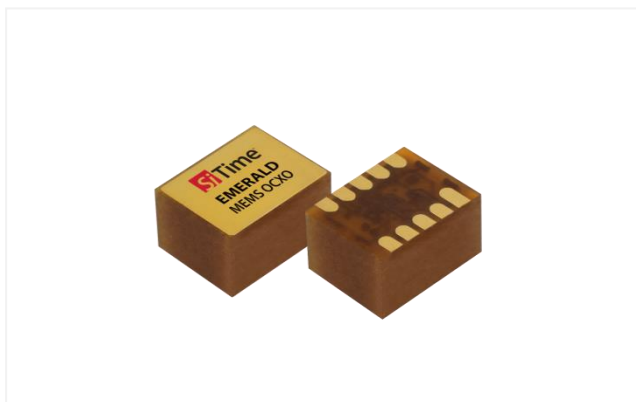


Figure 1. Top and bottom view

Package Pinout

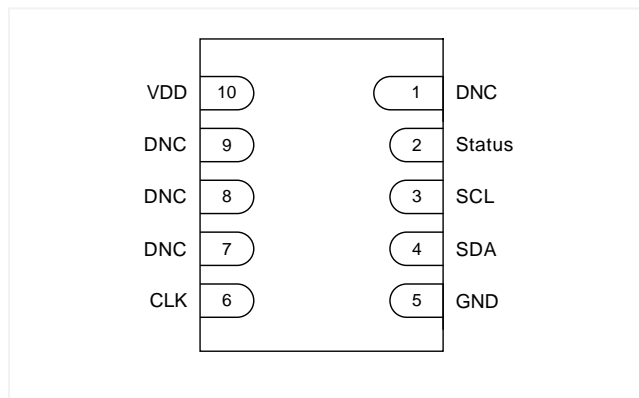
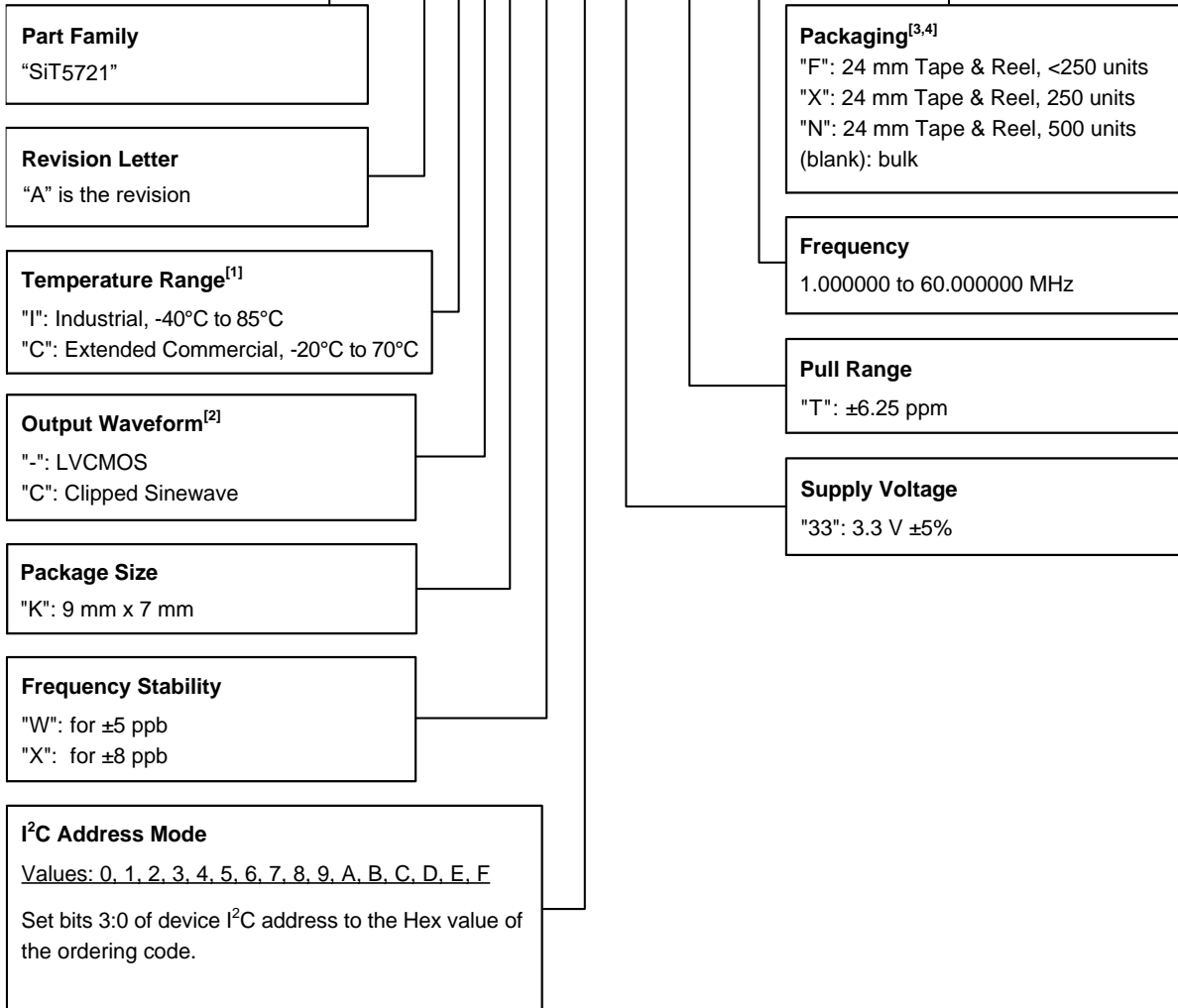


Figure 2. Pin Assignments (Bottom view)

Ordering Information

SiT5721AC-KW333-T-19.123456T



Notes:

1. [Contact SiTime](#) for other temperature range options.
2. "-" corresponds to the default rise/fall time for LVCMOS output as specified in [Table 2](#) (Output Characteristics). [Contact SiTime](#) for other rise/fall time options for best EMI.
3. Bulk is available for sampling only.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method^[4]

Device Size	12 mm T&R (<250 units)	12 mm T&R (250 units)	12 mm T&R (500 units)
9 mm x 7 mm	F	X	N

Note:

4. [Contact SiTime](#) for minimum order quantities for <250 units.

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Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 15 pF load unless otherwise stated.

Table 2. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	60	MHz	
Frequency Stability						
Frequency Stability over Temperature	F_stab	-5	–	+5	ppb	Referenced to (fmax + fmin)/2 over the specified temperature range. Contact SiTime for 3 ppb or tighter frequency stability.
		-8	–	+8	ppb	
Frequency vs. Temperature Slope	dF/dT	-0.12	±0.04	+0.12	ppb/°C	Steady airflow ≤3 m/s, 1°C/min ramp rate
Dynamic Frequency Change to Temperature Ramp	F_dynamic	-0.002	±0.0007	+0.002	ppb/s	Steady airflow ≤3 m/s, 1°C/min ramp rate
Initial Tolerance	F_init	-500	–	+500	ppb	Initial frequency offset at 48 hours after 2 reflows, measured at 25°C
Hysteresis Over Temperature	F_Hys	-0.8	±0.11	+0.8	ppb	Over -40 to 85°C, measured as maximum frequency deviation from center of hysteresis eye, 1°C/min ramp rate
One-day Aging	F_1d	–	±0.6	–	ppb	After 30-days operation, 50°C
One-month Aging	F_1m	–	±7	–	ppb	After 30-days operation, 50°C
One-year Aging	F_1y	–	±35	–	ppb	After 30-days operation, 50°C
Ten-year Aging	F_10y	–	±70	–	ppb	After 30-days operation, 50°C
Total Stability – 20 years	F_20y_stab	-1	–	+1	ppm	Better than Stratum 3E stability of ±4.6 ppm over 20 years per GR-1244-CORE. Inclusive of initial tolerance, frequency stability over temperature, 20-year Aging, and variations to supply voltage and output load. Typically called free running accuracy
Supply Voltage Sensitivity	F_Vdd	–	±0.3	–	ppb	VDD ±5%
Output Load Sensitivity	F_load	–	±0.2	–	ppb	LVC MOS output, 15 pF ±10%
		–	±0.2	–	ppb	Clipped sinewave output, 10 kΩ 10 pF ±10%
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse
OE Time	T_oe	–		680	ns	Time to first pulse after OE pin reaches 70% of VDD, 10 MHz
Warm-up Time	T_warmup	–	19.8	183	s	Time to within ±10 ppb of final frequency. Final frequency measured at one hour. 24 hours off prior to measurement.
		–	–	45	ms	Time to within ±200 ppb of final frequency. Final frequency measured at one hour. 24 hours off prior to measurement.
LVC MOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	2.4	3	ns	10% - 90% VDD
Output Voltage High – CLK Pin	VOH	90%	–	–	VDD	IOH = ±3 mA
Output Voltage Low – CLK Pin	VOL	–	–	10%	VDD	IOL = ±3 mA
Status Pin Output Characteristics						
Output Voltage High	VOH_P2	VDD-0.4	–	–	V	IOH = ±8 mA
Output Voltage Low	VOL_P2	–	–	0.4	V	IOL = ±8 mA
Clipped Sinewave Output Characteristics						
Output Voltage Level	V_OUT	0.8	–	1.2	V	Measured peak-to-peak swing at any VDD – 10 kΩ 10 pF ±10%
Rise/Fall Time	Tr, Tf	–	4.2	4.6	ns	20%–80% VOUT

Table 3. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	V _{DD}	3.14	3.3	3.47	V	Contact SiTime for other voltage options
Power Consumption						
Power Consumption – Warm-up	Pwr_warmup	–	–	2.3	W	Max power may be configurable lower, higher max gives shorter time
Power Consumption – Steady State	Pwr_steady	–	0.95	1.1	W	At +25°C
Temperature Range						
Operating Temperature Range	T _{use}	-20	–	+70	°C	Extended commercial
		-40	–	+85	°C	Industrial. Contact SiTime for -55°C and 95°C support

Table 4. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Tuning Range – I²C mode						
Pull Range	PR	±6.5	–	–	ppm	Contact SiTime for pull ranges up to ±3200 ppm
Absolute Pull Range ^[5]	APR	±5.5	–	–	ppm	
I²C Interface Characteristics ^[6]						
Bus Frequency	F _{I2C}	–	100	–	kHz	
		–	400	–	kHz	Contact SiTime for higher bus frequencies
Input Voltage Low	V _{IL_I2C}	–	–	30%	V _{DD}	
Input Voltage High	V _{IH_I2C}	70%	–	–	V _{DD}	
Output Voltage Low	V _{OL_I2C}	–	–	0.4	V	±20 mA
Output Fall Time	T _{f_I2C}			5	ns	70%–30% V _{OUT} , C = 50 pF
Input Leakage Current	I _L			650	nA	SDA pin, logic High
Pull-Up Equivalent Resistor	R _{PU}	25	40	55	kΩ	Internal pull up to V _{DD}
Input Capacitance	C _{IN}	–	6	–	pF	

Notes:

5. APR = PR – Total Stability.
6. I²C master must support clock stretching.

Table 5. Jitter & Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Period Jitter	T_jitt_per	–	1	–	ps	F_nom = 10 MHz, population 10k
RMS Phase Jitter (random)	T_phj	–	0.38	–	ps	F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
Allan Deviation						
$\tau = 1 \text{ second}$	AD_1s	–	2E-11	–		
$\tau = 10 \text{ seconds}$	AD_10s	–	1.5E-11	–		
$\tau = 100 \text{ seconds}$	AD_100s	–	1.5E-11	–		
Phase Noise						
1 Hz offset		–	-80	-76	dBc/Hz	Reference F_nom = 10.3 MHz
10 Hz offset		–	-109	-105	dBc/Hz	
100 Hz offset		–	-129	-126	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-153	-151	dBc/Hz	
100 kHz offset		–	-153	-150	dBc/Hz	
1 MHz offset		–	-165	-161	dBc/Hz	
5 MHz offset		–	-166	-160	dBc/Hz	

Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
V _{DD}	-0.5	4	V
Soldering Temperature (follow standard Pb-free soldering guidelines)	–	260	°C

Table 7. Environmental Compliance^[7]

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007, Condition A JEDEC JESD22-B103, Condition 1
Temperature Cycle	JESD22, MethodA104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL3
Washability	Non-washable

Note:

7. This device is RoHS and REACH compliant Pb-free and is Halogen-free and Antimony-free.

Pin-out Bottom View

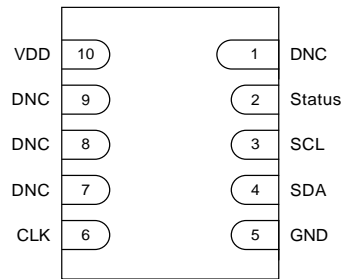


Figure 3. Size 9 mm x 7 mm

Table 8. Pin Assignments

Package Size	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
9 mm x 7 mm	DNC	Status	SCL	SDA	GND	CLK	DNC	DNC	DNC	VDD

Table 9. Pin Description

Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
DNC	DNC – Do Not Connect	-	Solder to pads, Do not connect
Status	Output	-	H: Device in normal operation L: Alarm, device not operating correctly
SCL	Input	-	I ² C Serial Clock Input ^[8]
SDA	Input/Output	-	I ² C Serial Data ^[8]
GND	Power	-	Connect to ground ^[9]
CLK	Output	-	LVC MOS, or clipped sinewave oscillator output
VDD	Power	-	Connect to VDD

Notes:

8. I²C address is a factory programmable option.
9. 0.1 μ F capacitor in parallel with a 10 μ F capacitor are required between VDD and GND.

Typical Performance Plots

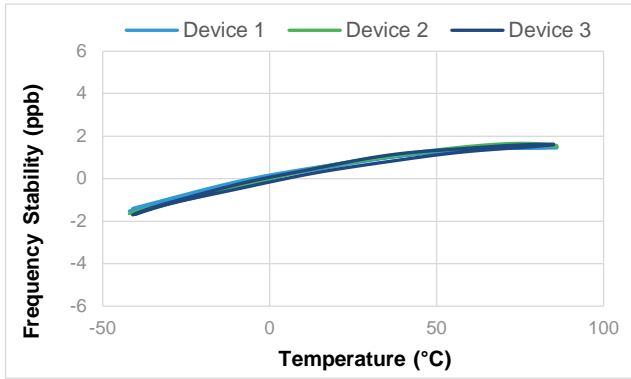


Figure 4. Frequency Stability

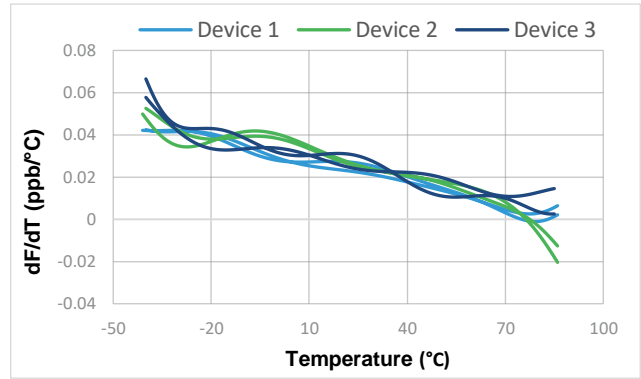


Figure 5. Frequency Slope

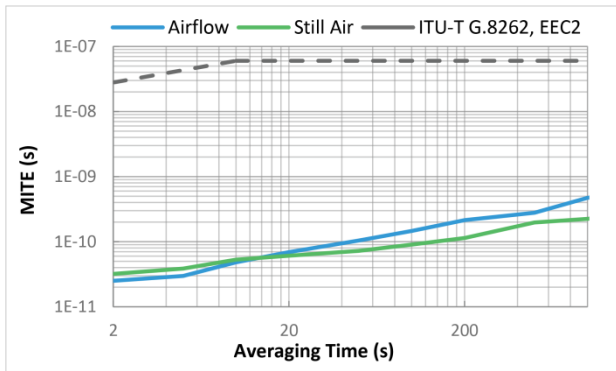


Figure 6. MTIE

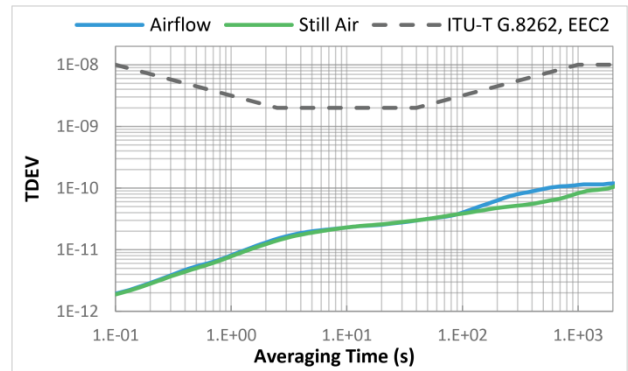
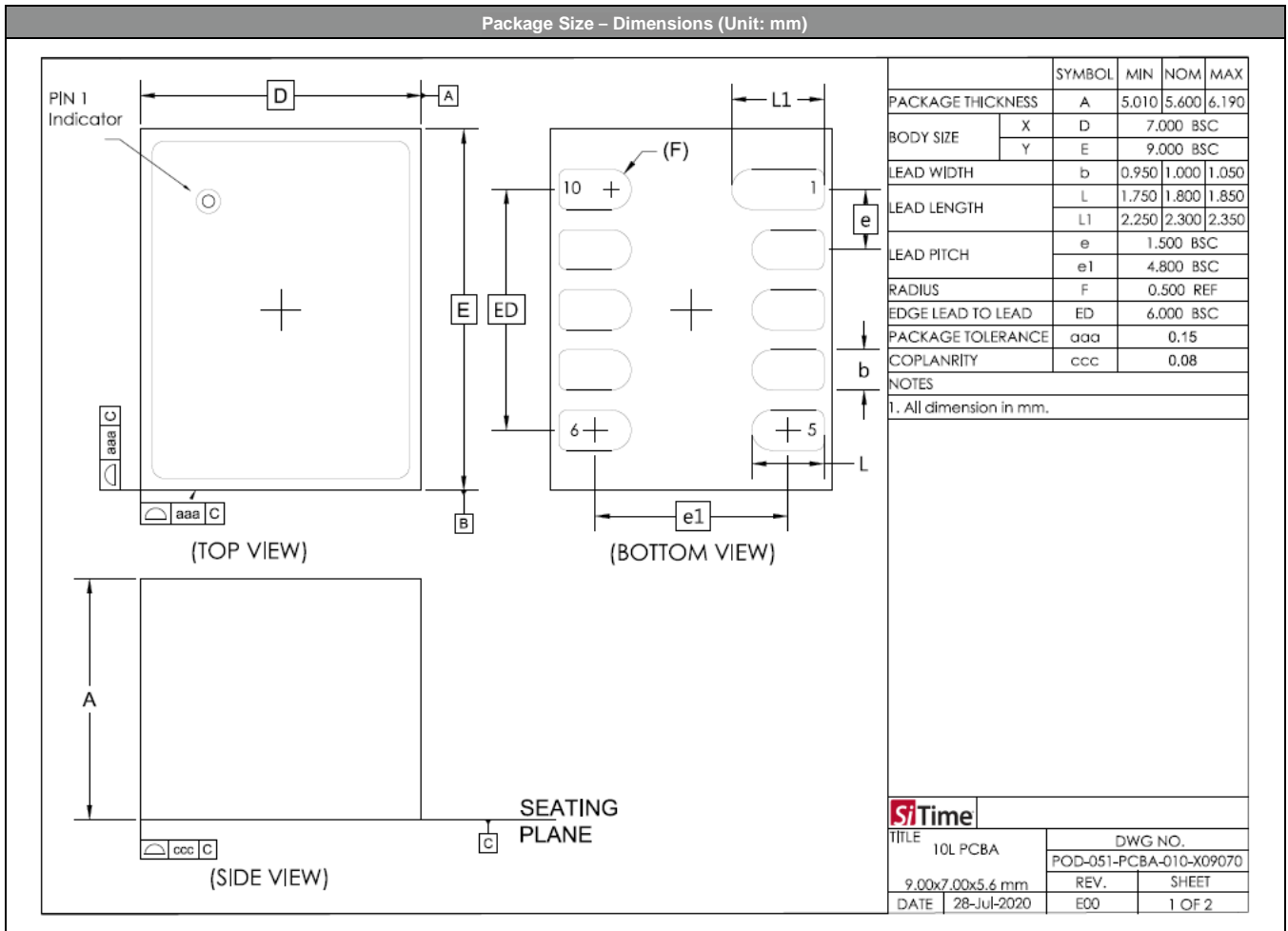


Figure 7. TDEV

Dimensions and Patterns — 9 mm x 7 mm package



Layout Guidelines

- SiT5721 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 μ F and 10 μ F). Place the bypass capacitors as close to the VDD pin as possible, typically within 1 to 2 mm. Ensure 0.1 μ F cap is placed closest to the device VDD and power pins.
- SiT5721 is engineered to have superior performance when compared to quartz OCXOs in the presence of ambient disturbers such as airflow and temperature transients. Therefore, the use of a metal cover typical for quartz OCXOs can often be avoided.
- It is recommended to connect all DNC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT5721 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, it is recommended to use “no clean” flux. Do not subject SiT5721 to liquid based cleaning processes.
- Reflow profile, per JESD22-A113D.
- For additional manufacturing guidelines and marking/tape-reel instructions, refer to [SiTime Manufacturing Notes](#).

Table 10. Additional Information

Document	Description
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.
SiT6731 EVB	Evaluation board, contact SiTime
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info
Qualification Reports	RoHS report, Reliability reports, Composition reports
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies
Termination Techniques	Termination design recommendations
Layout Techniques	Layout recommendations
Other Quality Documents	ISO certificate, materials declarations, environmental policy, warranty on date code

Table 11. Revision History

Version	Release Date	Change Summary
0.83	09/17/2019	First release, preliminary information
0.84	10/30/2019	Changed Rise/Fall time condition for Clipped Sinewave Output Characteristics Other minor changes
0.85	04/20/2020	Updated various specifications and conditions after characterization Updated package drawings and pinouts view
0.9	08/10/2020	Added Appendix: Emerald™ DCOCXO Programming Guide Updated ordering information

Appendix

Introduction

This programming guide is applicable to SiTime's Emerald digitally controlled OCXO (DCOCXO). It provides system developers with the necessary design information including I²C interface timing, I²C data format, register definition and register read/write access.

The SiT5721 (1 to 60 MHz) Emerald DCOCXO supports unique features such as

- Digital frequency pulling with ± 5 ppt resolution
- Adjust frequency-pull ramp rate
- Temperature read-back
- Error status flag

These features allow system designers to enhance system robustness by eliminating output frequency sensitivity to board level noise and enabling device status monitoring. By reading and writing to the registers through the I²C interface, the guide supports designers in utilizing the distinct features SiT5721 has to offer, including adjusting frequency pull and ramp rate, reading temperature, and checking error status flags.

Register Definitions and Descriptions

SiT5721 provides three categories of registers with read/write accessibility via I²C:

- **Description Registers** – read only registers that provide information about the specific part.
- **Control Registers** – read/write registers that allow for controlling the behavior of the part.
- **Status Registers** – read only registers that provide current operating values of the part.

The details of these registers are defined in the following sections. Many of the registers use a single precision floating point (binary 32 IEEE 754-2008 standard) data type. Details on the float point approach can be found in [Floating Point Interface](#) section.

Examples of writing and reading registers can be found in [I²C Read and Write Example](#) section.

Refer to the SiT5721 datasheet for other device information such as pin map and description, electrical spec and package dimensions.

Description Registers

Description Registers (1024 Byte Block)						
Register Address	Name	Size (bytes)	Format	Units	Read/Write	Default
0x50	Part Number	256	ASCII	-	R	Factory Set
0x51	Reserved	-	-	-	-	-
0x52	Nominal Frequency	32	ASCII	MHz	R	Factory Set
0x53	Reserved	-	-	-	-	-
0x54	Reserved	-	-	-	-	-
0x55	Reserved	-	-	-	-	-
0x56	Reserved	-	-	-	-	-
0x57	Reserved	-	-	-	-	-

Each of the header registers returns ASCII values representing the header attribute (e.g. Part Number = "SiT5721AC-KW333JT-19.123456T"). The first returned byte that is equal to 0 indicates the end of the ASCII string.

Control Registers

The SiT5721 DCOCXO enables control of the frequency pull and maximum frequency-pull ramp rate. The following table defines the locations and parameters of each register.

Control Registers (1024 Byte Block)						
Register Address	Name	Size (bytes)	Format	Units	Read/Write	Default
0x60	Reserved	-	-	-	-	-
0x61	Pull Value	4	Float	Fractional Offset	R/W	0
0x62	Pull Range	4	Float	± Fractional Offset	R/W	6.5E-06
0x63	Reserved	-	-	-	-	-
0x64	Max. Frequency Ramp Rate	4	Float	Fraction/Second	R/W	1.00E-05
0x65	Reserved	-	-	-	-	-
0x66	Reserved	-	-	-	-	-
0x67	Reserved	-	-	-	-	-
0x68	Reserved	-	-	-	-	-
0x69	Reserved	-	-	-	-	-
0x6A	Reserved	-	-	-	-	-
0x6B	Reserved	-	-	-	-	-
0x6C	Reserved	-	-	-	-	-
0x6D	Reserved	-	-	-	-	-
0x6E	Reserved	-	-	-	-	-
0x6F	Reserved	-	-	-	-	-

Pull Value:

The pull value is the adjustment that the designer desires to make to the factory programmed center frequency, where the center frequency is the device frequency with the Pull Value set to 0. It is a fractional offset in the form of a 32-bit float. For a desired shift of +1 ppm, the designer would write the value of 1.00E-06 to the register address 0x61. A desired shift of 1 ppm lower than the factory programmed frequency would be entered into the register as -1.00E-06. However, the set pull value is not persistent; the output will return to the factory programmed frequency during power cycles. The designer can read from as well as write to this register and the factory default is no frequency offset.

Pull Range:

The pull range is the limit above and below the center frequency to which the center frequency can be pulled. The default for this register is 6.5 ppm and the designer can adjust the pull range lower to establish a narrower acceptable pull value. This value and any value written to this register are absolute; it is the value in the register above and below zero. For example, if the designer writes 3.0E-06 to the register, the pull range would be -3E-06 to +3E-06 relative to the center frequency. The designer can read from and write to this register.

Maximum Frequency Ramp Rate:

The maximum frequency ramp rate is the maximum rate at which the output frequency will adjust until it meets the set pull value or hits the set pull range. It is a 32-bit float which is set in the unit of fraction per second. The maximum rate that can be set is 10 ppm/second, which is the default. As an example, if the designer needs the maximum ramp rate to be 1 ppm/second, they would write 1.00E-06 to the register address 0x64.

Status Registers

Status registers are used to monitor the operation of the Emerald. Status registers that can be read are the time since start register, resonator temperature register, and the error status flag. All status registers are read only and updated at 1 kHz.

Status Registers (512 Byte Block)					
Register Address	Name	Size (bytes)	Format	Units	Read/Write
0xA0	Time Since Power Up	4	Unsigned Int.	Seconds	R
0xA1	Resonator Temperature	4	Float	Degrees C	R
0xA2	Reserved	-	-	-	-
0xA3	Reserved	-	-	-	-
0xA4	Reserved	-	-	-	-
0xA5	Reserved	-	-	-	-
0xA6	Reserved	-	-	-	-
0xA7	Reserved	-	-	-	-
0xA8	Reserved	-	-	-	-
0xA9	Reserved	-	-	-	-
0xAA	Reserved	-	-	-	-
0xAB	Reserved	-	-	-	-
0xAC	Reserved	-	-	-	-
0xAD	Reserved	-	-	-	-
0xAE	Error Status Flag	4	Unsigned Int.	Bit Field	R

Error Status Flag:

The Error Status Flag alerts the user of any errors during operation. If the register reads the value 7, the device is in normal operation. If any other values are read, [contact SiTime](#). Along with the Error Status Flag register, Pin 2 indicates error status. While this pin is voltage high, the device is in normal operation.

Error Status Pin:

Along with the Error Status Flag register, Pin 2 indicates error status. While this pin is voltage high, the device is in normal operation.

I²C Interface Configuration Description

Serial Interface Configuration Description

Emerald includes an I²C interface to access registers that control the DCOCXO frequency pull range, and frequency pull value. The SiT5721 I²C is a slave-only interface with clock stretch and clock speeds up to 400 kHz. Emerald, during the transaction, can hold SCL LOW to force the master into a wait state until it has performed internal operations. Therefore, clock stretching support by the master is required. The I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. [Figure 8](#) shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in [Figure 9](#)).

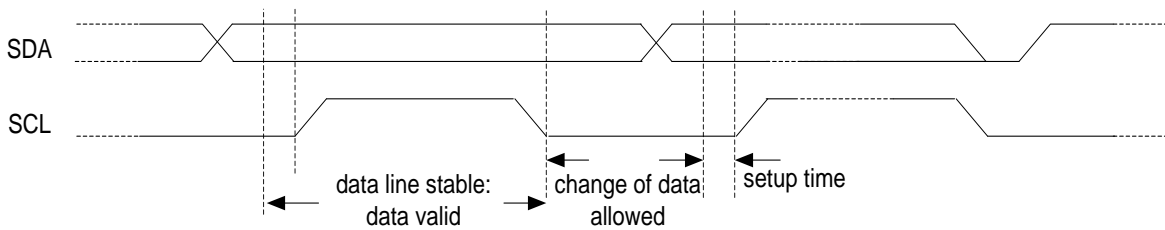


Figure 8. Data and clock timing relation in I²C bus

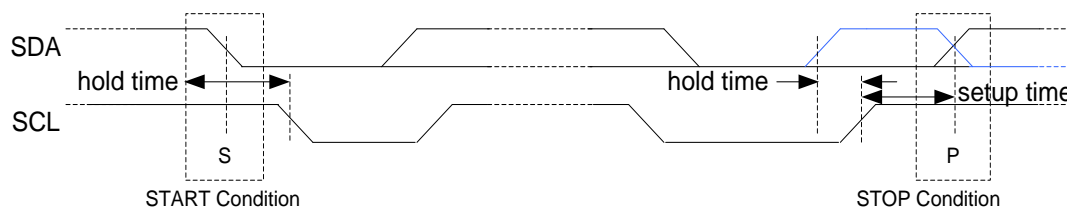


Figure 9. START and STOP (or repeated START, blue line) condition

Byte Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is defined by the address being written. Data is transferred with the LSB (Least Significant Byte) first. The detailed data transfer format is shown in [Figure 11](#) below.

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received, and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from Emerald is when the transmitted address does not match the slave address. When the master is reading data from the device, SiT5721 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START.

Data Format

This I²C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and “1” indicates a read transaction and a “0” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (0x00 to 0xFF). Auto register address incrementing is supported for read operation only and within one register group. This allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. The data format is based on the register being accessed (ASCII, 32 bit float, 32 bit ints). Float and Int values are set least significant byte first (little endian).

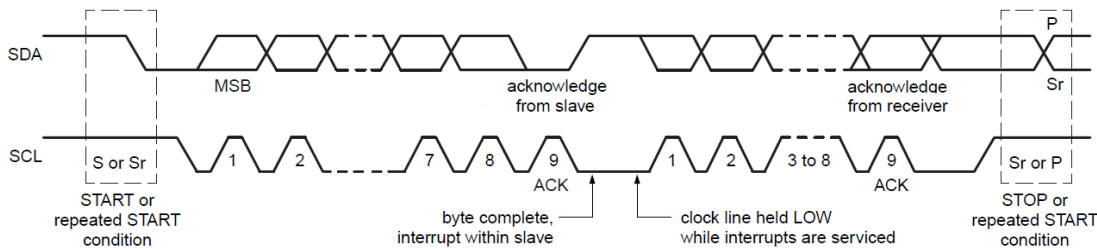


Figure 10. Parallel signaling format

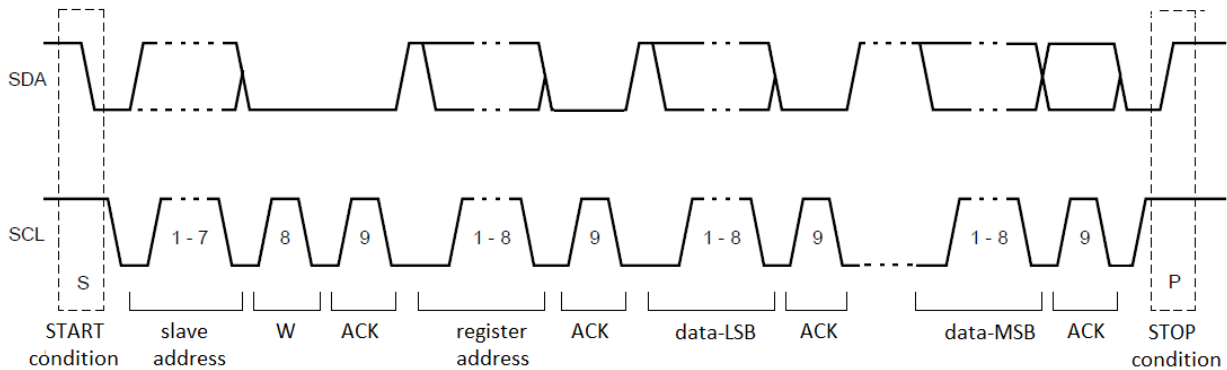


Figure 11. Parallel data byte format, write operation

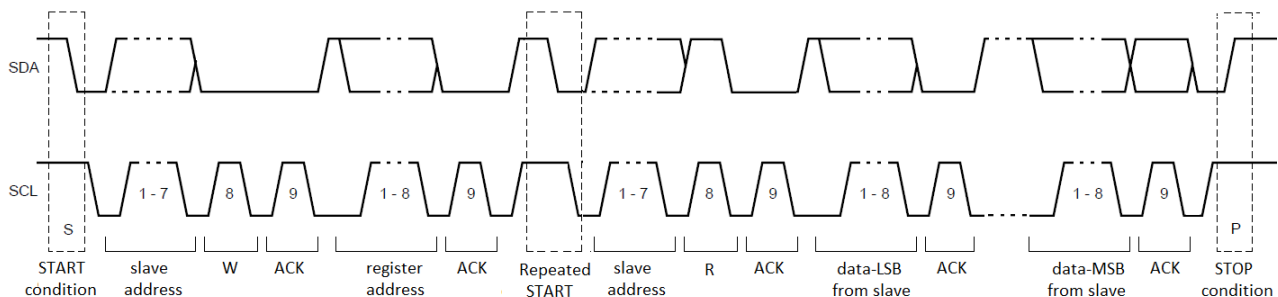


Figure 12. Parallel data byte format, read operation

I²C Timing Specification

The below timing diagram and Table 12 illustrate the timing relationships for both master and slave.

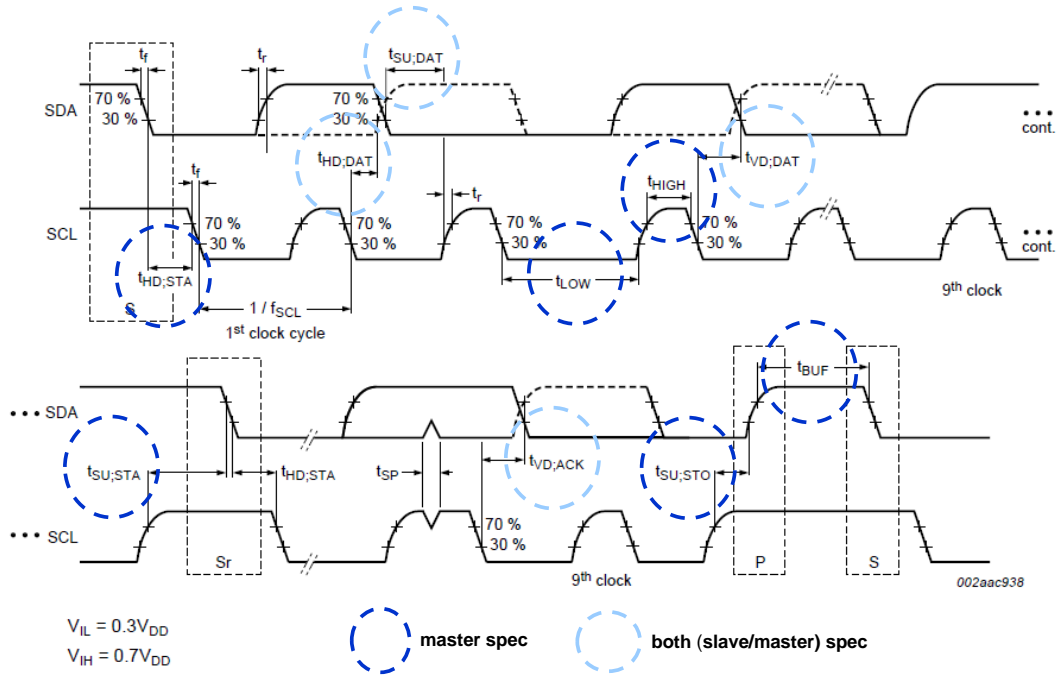


Figure 13. I²C Timing Diagram

Table 12. I²C Timing Requirements for Fast Mode (FM) and Standard Mode (SM)

Parameter	Speed Mode	Minimum Value	Unit
$t_{SU,DAT}$	FM (400 KHz)	>100	ns
	SM (100 KHz)	>250	ns
$t_{HD,DAT}$	FM (400 KHz)	>0	ns
	SM (100 KHz)	>0	ns

Programming Guide and Examples

This section of the document provides a guide on how to program SiT5721. The first subsection provides details on floating point numbers and how to convert between binary and floating point. The second subsection describes how to use the floating point interface to communicate the desired frequency pull. Finally, the last subsection provides examples of how to read to and write from the SiT5721 registers.

Floating Point Interface

Emerald uses 32-bit single precision floating-point numbers for some of the register values as specified by IEEE-754-2008 and repeated below for convenience:



Bit 31 is the sign bit with the following definition:

0 = Positive number
1 = Negative Number

Bits 30:23 contain the exponent value and bits 22:0 contain the fractional value.

The conversion formula to decimal in normalized form is:

$$= (-1)^S \times (1 + Fraction) \times 2^{(Exponent-127)}$$

The normalized form is used to express most values except 0. As an example, if:

- S = 1b
- Exponent = 1000 0010b
- Fraction = 011 1000 0000 0000 0000 0000b

Then the binary fraction would be converted to decimal:

$$011\ 1000\ 0000\ 0000\ 0000\ 0000b = \frac{0}{2^1} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} \\ = 0.4375d$$

Similarly, the exponent would be converted to decimal:

$$1000\ 0010b = 2^1 + 2^7 = 130d$$

Finally, by substituting the calculated values into the formula provide above, the total decimal value would be:

$$= (-1)^1 \times (1 + 0.4375) \times 2^{(130-127)} = (-1) \times 1.4375 \times 2^3 = -11.5d$$

Frequency Control Using Floating Point Numbers

To clarify how the frequency control operates, the floating-point value sets the offset in fractional frequency units. For instance, +1.00e-6 is 1.00 ppm higher frequency shift, and -1.23456e-9 is 1.23456 ppb lower frequency. These values must be written to the control registers using the proper IEEE-754-2008 format described in [Floating Point Interface](#) section.

The fractional part of the single-precision floating point number (mantissa) is 23 bits and the frequency resolution is therefore 1 part in 2^{23} , or approximately 0.000,000,12. The following two examples demonstrate a couple of frequency resolution cases.

Frequency Pull Value	Resolution of Pull Value
5 ppm	0.6 ppt
0.1 ppm	0.01 ppt

These values are below the Emerald noise floor and therefore do not contribute additional noise.

I²C Read and Write Example

The address of the part is based on the part number that was ordered.

SiT5721 AC-KW333JT-19.123456T

I²C Address Mode
 Values: 0, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
 Set bits 3:0 of device I²C address to the Hex value of the ordering code. When the I²C address is factory programmed using these codes, pin A0 is NC.

I ² C Address Ordering Code	Device I ² C Address
0	1100000 (0x60)
1	1100001 (0x61)
2	1100010 (0x62)
3	1100011 (0x63)
4	1100100 (0x64)
5	1100101 (0x65)
6	1100110 (0x66)
7	1100111 (0x67)
8	1101000 (0x68)
9	1101001 (0x69)
A	1101010 (0x6A)
B	1101011 (0x6B)
C	1101100 (0x6C)
D	1101101 (0x6D)
E	1101110 (0x6E)
F	1101111 (0x6F)

Values of format type float and integers are sent in little endian format (MSB last).

Example Read Description Register

Emerald provides a register based I²C interface for accessing data from the device. The description, status, and control registers can all be read. Data is returned in the size and format listed in the table for each register. The address associated with SiT5721 is based on the part number that was ordered. The sequence to read an I²C register is to first write the register number to the SiT5721 I²C address and then read back the data from the same address (read/write transaction).

Read Nominal Frequency Example:

- SiT5721 I²C order code: 2 – converts to I²C slave address of 0x62
- Register read: Nominal Frequency – register 0x52
- Master write:
 - Write address 0x62
 - Data: 0x52
 - Stop
- Master read:
 - Read address 0x62
 - Read 32 bytes
 - SiT5721 returns “20.000000MHz” (followed by 0x00 24 times)
 - Stop

Write Control Register Example

The control registers of the I²C interface are writable for changing operating parameters in the Emerald. Data size and format are listed in the control register table.

Example Write Pull Value

- Emerald I2C order code: 4 – converts to I2C slave address of 0x64
- Register read: Pull Value – register 0x61
- Value: Change frequency by +1 ppm. In floating point this is +1.00e-6, which as a 32 bit float is 0x358637BD.
- Master write:
 - Write address 0x64
 - Data: 0x61 (register), followed by 0xBD 0x37 0x86 0x35 (little endian send of 1.00e-6)
 - Stop

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